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# Recent Progress on Negative Capacitance Tunnel FET for Low-Power Applications: Device Perspective

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**Abstract**

In the present-day scenario of low-power electronics, there is a steady and increasing need for an adequate device that can counteract the power dissipation issue due to the consistent scaling of device dimensions. For this purpose, the evolution of low subthreshold swing (SS) based devices, especially with the negative capacitance (NC) techniques, has presented a well-favored solution. The NC of ferroelectrics (FE) materials could **be** widely utilized to provide the gate voltage ($V_G$) amplification under specific conditions to boost the performance of the MOS device, by addressing the ultimate fundamental limitation of Boltzmann Tyranny and offering the SS much lower than $60mV/dec$. Along with the advent of this state-of-art NC technology, tunnel field-effect transistor (TFET) also emerges for accomplishing low SS and becomes one of the promising techniques for low-power applications. Incorporating these two principles (NC and tunneling) into a single device architecture enables the super-steep SS and remarkably low OFF current ($I_{OFF}$). This cutting-edge combination, negative

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capacitance tunnel FET (NC-TFET) device has opened up the possibility of an ultra-low-power and high-performance device. This review paper mainly focuses on the theoretical background and recent progress in the field of NC-TFET with abundant quantum-mechanical models and various perspectives such as transistor perspective, analog circuit perspective, and future road map perspective.

*Keywords:* Negative Capacitance, NC–Tunnel FET, low power electronics, subthreshold swing, voltage pinning.

## 1. Introduction

In the modern era, consumer electronic devices like phones, smartwatches, and tablet PCs require deeply scaled, high-speed, and ultra-low power transistors. To achieve the high packing density, the device dimension of transistors must be scaled down according to the Dennard scaling rule [1]. This leads to several deterioration short channel effects (SCEs) like threshold voltage ($V_{Th}$) roll-off, drain and gate induced barrier lowering (D/GIBL), etc. However, to reduce the overall power consumption of the device, it is important to operate the device at a lower supply voltage, without affecting the overall device performance. The high value of ON-OFF current ratio ($I_{ON}/I_{OFF}$) can be achieved by reducing the subthreshold swing ($SS$) .

The $SS$ is defined as the inverse of the subthreshold slope curve, and is given as [2]-[79]

$$SS = \left[\frac{\partial(\log_{10} I_D)}{\partial V_G}\right]^{-1} = \left[\frac{\partial \psi_S}{\partial V_G} \times \frac{\partial(\log_{10} I_D)}{\partial \psi_S}\right]^{-1} \tag{1}$$

where $V_G$ is the gate voltage, $\psi_S$ is the surface potential, and $I_D$ is the current due to the thermionic injection of carriers from source to channel is given as [4],[5]

$$I_D = I_0(e^{q\psi_S/k_BT} - 1) \tag{2}$$

The (1) shows that the $SS$ is associated with the transport and body factor. The transport factor ($n^{-1} = \partial\psi_S/\partial \log_{10} I_D$), using (1), $n = \frac{q \log_{10} e}{k_B T} = 60mV/dec.$. The body factor ($m$) ($m^{-1} = \partial\psi_S/\partial V_G = (1 + C_{Device}/C_{ox})^{-1}$ is always greater



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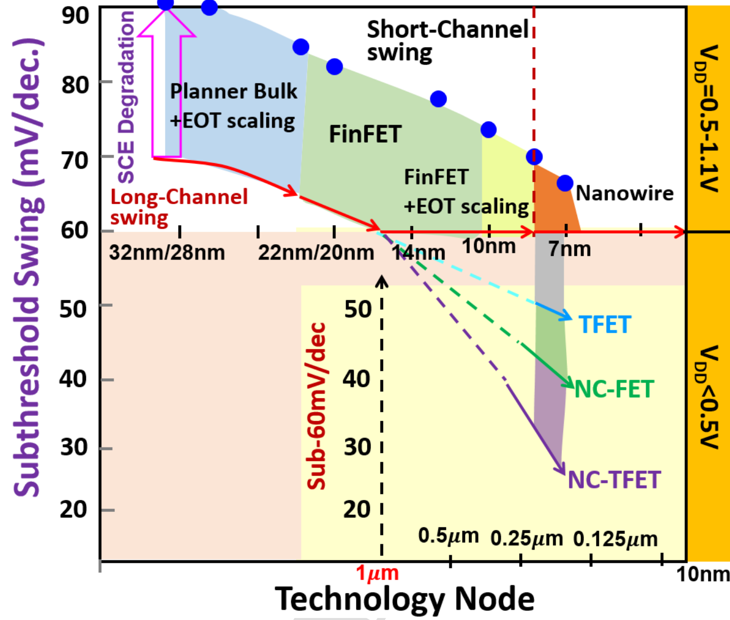


Figure 1: Graphical representation of comparison among the conventional and non-conventional devices in terms of the SS and supply voltage (which is a major factor of power dissipation). The figure is just a pictorial summary of low-power steep-$SS$ devices)

than one, where $C_{Device}$ is baseline device capacitance and $C_{ox}$ is the oxide capacitance.

The non-planer MOS transistors, like FinFET, gate all around (GAA) FET, nanowire (NW) FET, etc. have been widely researched [6]-[13]. These devices offer a better scaling, and superior gate electrostatic than the planer MOS device, and are capable enough to mitigate several short-channel effects (SCEs). However, the current conduction in these devices is due to the thermionic injection of charge carriers by overcoming the energy barrier. This will limit the steepness of the subthreshold slope. Hence the overall $SS$ of a conventional MOS device is always greater than the $60mV/dec.$ (as shown in Fig. 1), which is also known as *Boltzmann Tyranny*.

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This so-called *Boltzmann Tyranny* is mainly dependent upon two factors: 1) body factor and 2) transport factor. This issue is mitigated either by optimizing the transport factor or body factor [14],[15]. To push the limit of body factor, the devices like Micro-Electro-Mechanical-Systems (MEMS) based FET or Suspended-Gate (SG) MOSFET (SG-MOSFET), and negative capacitance (NC) FETs have been extensively studied, and researched by various academic and scientific groups. The SG-MOSFET requires high voltage, which cannot be in favor of the low power integrated circuits (ICs) [17]. However, in NCFET, the ferroelectric (FE) capacitor is placed in a series of gate oxide capacitance, which will offer voltage amplification. The presence of the FE layer causes a reduction in the body factor and results in a lower value of $SS$ than the fundamental limit of a conventional MOS device.

However, another technique to reduce the $SS$ is transport factor reduction, which is lowered by employing the different carrier injection mechanisms. For that purpose devices like impact-ionization MOS (I-MOS), and Tunnel FETs (TFETs) have been proposed. The I-MOS uses the concept of modulation of the avalanche breakdown voltage to switch ON or OFF the device [18]. However, the TFET uses quantum mechanical band-to-band tunneling (BTBT). Undoubtedly, this carrier injection technique effectively reduces the SS lower than the $60mV/dec$. However, given the fact that the TFETs suffer from lower $I_{ON}$ and ambipolar conduction issues [19], [20].

Therefore, in order to achieve a sufficiently low $SS$, $I_{OFF}$ and high $I_{ON}$, one should co-integrate the NC concept and BTBT concept together, resulting in a device called, Negative Capacitance-Tunnel FET (NC-TFET). The NC and BTBT concepts are simultaneously used to boost the device performance by optimizing both (body, and transport) factors at the same time.

With the fact that both the body factor and transport factor are concurrently involved to ensure the lower value of SS in NC-TFET devices. Several experimental and theoretical investigations have been done on NC-based TFET devices. The Lee et. Al. has experimentally integrated the FE layer into the gate stack of NC concept in the planner TFETs device. Furthermore, the

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stacking of FE layer into the gate stack is also experimentally done for different TFETs devices like hetero-tunnel FET (HTFETs), nanowire TFETs (NWT-FETs) device to achieve the superior performance [21]-[30]. To further improve the performance the different nonplanner device architectures like double gate [31], gate all around (GAA) [32], T-shaped gate [33], L-shaped gate [34], and vertical tunneling [35]-[37] based NC-TFET have been studied based on the TCAD simulation. These devices ensure the better performance of the NC-TFET device by ensuring better electrostatic control and increasing the area of the line tunneling without changing the device dimensions. Apart from this, the channel doping, advanced and 2D materials-based channel is also explored theoretically to further improve the overall device performance of NC-based TFETs [38]-[41]. No doubt, a perfectly matched NC will have the internal voltage amplification, which will further add the additional energy band bending, and enhance the BTBT probability. This results in appreciable enhancement in the performance of Tunnel FET in terms of high ON current and low ambipolar conduction. Consequently, the key concept of having the lower SS, higher $I_{ON}$, and hysteresis-free operation in NC-TFET is achieved by the proper matching of $C_{FE}$ with $C_{ox}$ i.e. $|C_{FE}| \approx C_{ox}$.

The main objective of this review paper is to provide a detailed theoretical and mathematical discussion of the existing literature on NC-TFETs. Additionally, usage of the NC concept in TFETs provides a better understanding of the recent trends in low-power analog and digital circuits.

The organization of this paper is as follows: Section 1 introduces in detail the major obstacle faces by the conventional and non-conventional MOS devices, and also briefly introduces the technical background of negative capacitance and NC-TFET technology. Section 2 gives the detailed physics of the Negative capacitance effect and how it has been used in FETs. Section 3 provides insight into stabilizing the negative capacitance and discusses the different techniques to stabilize negative capacitance. In Section 4, we have discussed the principal and operations of NCFET. Herein, is a detailed overview of how ferroelectric materials are being employed to obtain the negative capacitance-induced effect

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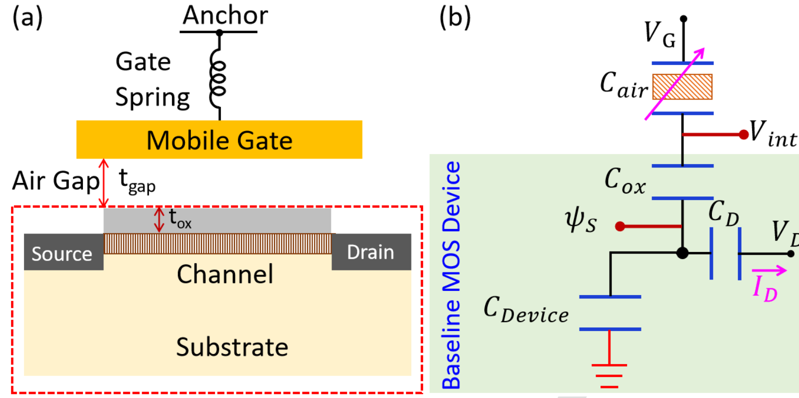


Figure 2: (a) Schematic of the Suspended-Gate MOSFET including the mobile conductive gate (with k equivalent mechanical spring constant) over air/oxide/semiconductor, and (b) capacitor divider circuit model.

in FETs. Section 5 presents a detailed discussion of the modeling approaches for the NCFET. The detailed discussion of the principal and operation of the different NC-TFET structures and their application in analog/RF and digital circuits are discussed in detail in sections 6, 7, and 8 respectively. In section 9 we have listed research and development-related concerns of NC-TFET. Finally, we conclude our review work by listing the future scope of NC-TFET based on the materials, device architecture, circuits, and system.

## 2. Negative Capacitance

In common parallel plate capacitors, the charge ($Q$) on either side of the plate is directly proportional to the applied voltages ($V$) on the terminals [42], [43]

$$Q = C \cdot V \tag{3}$$

where $C$ is the proportionality constant, called capacitance.

However, the term *"negative"* in negative capacitance means, that when there is an increase in voltage, leads to a decrease in charge or vice-versa [44].

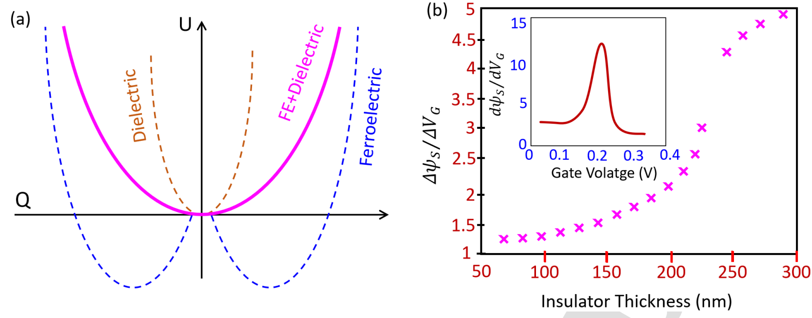


Figure 3: (a) Energy ($U$) vs charge ($Q$) characteristics for the gate stack having insulating layer of dielectric or FE or FE-dielectric. (b) Voltage gain ($\partial\psi_S/\partial V_G$) vs dielectric thickness.

For a better understanding of negative capacitance, take the example of SG-MOSFET, in which the MEMS functionality is added in solid state principle [17].

The fact that SG-MOSFET has the suspended metal gate or mobile gate over the oxide layer of the MOS device is supported by the gate spring, as shown in Fig. 2 (a). At $V_G = 0$, leads the air gap between the mobile gate and oxide layer, causing the capacitance ($C_{air} = 0$) between the mobile gate and oxide layer, which makes the transistor switched OFF. Applying the gate voltage, the electro-mechanical action takes place, due to which the mobile gate deflects towards the oxide layer, leading to a decrease in $C_{air} = 0$. At $C_{air} = 0$ (i.e., the mobile gate in contact with the oxide layer), the channel inversion is achieved, due to an increase in the gate-to-channel capacitance. The SG-MOSFET is a high voltage (HV) device, designed and developed to achieve a subthreshold swing lower than $60mV/dec.$ [45].

## 3. Stabilised Negative Capacitance

The hysteresis characteristics of FE materials are the major obstacle to the use of NCFETs in logic applications. The Fig. 3(a) portrays the energy ($U$) vs. charge ($Q$) plots for three different cases: 1) For the dielectric capacitor, 2)



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FE capacitor, 3) and the "dielectric + FE" capacitor. Herein, the FE capacitor is connected in series with the dielectric capacitor. When two capacitors are connected in series, the magenta-colored $U$ vs. $Q$ curve can be introduced (see Fig. 3 (a)), which is said to be the capacitance-matching state of the total capacitance has the minimum energy at the origin point [46], [47]. In order to achieve the stable operation of NCFET, there is a need for capacitance matching, which can be achieved by the two approaches: 1) FE layer scaling, 2) optimization of base-line device capacitance [43],[48].

### *3.1. Ferroelectric Layer Scaling*

To understand it, consider the metal-insulator–FE–metal capacitor structure. The total energy ($U_{Total}$) is consisting of the sum of the free energy of dielectric ($U_D$) and FE ($U_{FE}$) layers.

The $U_D$ (per area) is given by [43].

$$U_{ox} = \frac{P^2}{2\epsilon_0 \epsilon_{ox}} \tag{4}$$

where $\epsilon_0$, and $\epsilon_{ox}$ are the vacuum and dielectric permittivity respectively.

The $U_{FE}$ (per area) is [43]

$$U_{FE} = \alpha P^2 + \beta P^4 + \gamma P^6 - E \cdot P + K(\nabla P)^2 \tag{5}$$

where, $\alpha, \beta$, and $\gamma$ are called Landau coefficients, their values are listed in [49].

Below *Curie* temperature, $\alpha$ has a negative value, which results in the hysteresis characteristics in FE materials. $E$ is the electric field. The term $-E \cdot P$ in (5) is the electrostatic energy, and $K$ is the domain coupling constant. $K(\nabla P)^2$ is the Ginzburg term, which will be ignored during the formulation of $P$–$V_{FE}$ relation [50].

Now, total free energy (per area) is given as

$$U_{Total} = U_D \cdot T_{ox} + U_{FE} \cdot T_{FE} \tag{6}$$

where, $T_{ox}$ and $T_{FE}$ is the thickness of oxide and FE layers respectively.

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Using (4) and (5) in (6), and having some algebraic manipulation we have,

$$U_{Total} = \left[\frac{T_{ox}}{2\epsilon_0\epsilon_{ox}} + \alpha T_{FE}\right] P^2 + T_{FE}\left[\beta P^4 + \gamma P^6\right] - V \cdot P + k(\nabla P)^2 \quad (7)$$

To achieve the stabilized NC the first term in bracket on right hand side of (7), must have the positive value i.e.

$$T_{FE} \leq T_{FE,crtcl} = \frac{T_{ox}}{2\alpha\epsilon_0\epsilon_{ox}} \quad (8)$$

where symbols have their usual meanings.

For clear understanding consider the Fig. 3(b), where the voltage gain ($\Delta\psi_S/\Delta V_G$) increases with respect to the oxide layer thickness and has more steeper curve at $250nm$ [51]. The $\Delta\psi_S/\Delta V_G = 4$ achieved for $T_{ox} = 250nm$ and change in gate voltage ($\Delta V_G$) from 0 to $0.2V$ (shown in Fig. 3(b) insect). The voltage gain ($\Delta\psi_S/\Delta V_G = 4$) ensure the change in surface potential ($\Delta\psi_S = 0.8V$) for applied $V_G = 0.2V$.

So, in order to ensure a stable NC, and better voltage amplification, one should ensure that either $C_{FE}$ must be large or $C_{ox}$ must be small enough. For this purpose, it is necessary to select the FE layer of optimized thickness, which results in the optimal value of ferroelectric capacitance. It is indispensable for the low SS steep switching, and hysteresis-free NCFET [52]. To utilize the impacts of NC in NC-TFET devices, capacitance matching is quite essential. To the best of our knowledge, fabricated, modeled, and TCAD simulated NC-TFET device structures, the FE layer scaling approach is frequently applied to achieve the stabilized NC operation [21]-[41].

### *3.2. Base-Line Capacitance Optimization*

The second technique is to achieve capacitance matching and hysteresis-free operations by optimization of baseline capacitance. For this purpose, the optimum value of device dimension and drain voltage baseline device. There is a trade-off between the hysteresis window and the sub-threshold slope of the device. The hysteresis-free state on NCFET has degraded device performance. For this purpose Ko et. al. optimized the source/drain extension length ($L_{ext}$) to

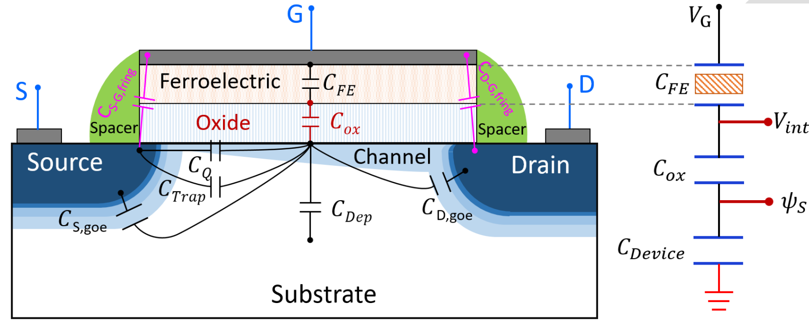


Figure 4: Schematic view of bulk NC-FET, and the capacitors associated with the FE layer, oxide, spacers, channel, trap, source/drain junction, and baseline device.

ensure the adequate value of gate-source/drain capacitance ($C_{GS}/C_{GD}$), which will ensure the narrow hysteresis window. However, the dependence of drain voltage on hysteresis window has been observed experimentally in [46]. It has also been proven that at high drain voltage, large hysteresis occurs, which shows the impact of drain voltage on the charge-balance with the ferroelectric capacitor [46],[53],[54].

However, there is no discussion found in the literature on NC-TFET, where capacitance matching is achieved by the optimization of the baseline capacitance for NC-TFET devices. This is due to the design and fabrication guidelines of TFET devices. The TFET device has different polar characteristics for the source/drain region. Also, channel surface potentials in the sub-threshold condition are different in TFET in comparison to the MOS device. These differences change capacitance distribution in a device. In addition, TFET device structure and material have huge variations. For example, device designs with vertical tunneling, L-shaped, and special gate stack structure are proposed. Also, a hetero-tunnel junction is often used.

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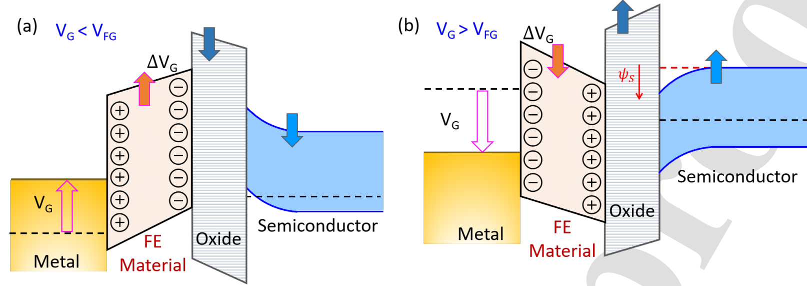


Figure 5: Band bending in NCFET (a) for $V_G < V_{FB}$, and (b) for $V_G > V_{FB}$.

### 4. NCFET: Principal & Operation

The power dissipation in the MOS device will be significantly reduced by operating the device at a lower operating voltage. However, the *Boltzmann Tyranny* has put a limitation to operate the highly scaled MOS devices at lower voltages. The $SS$ (inverse of subthreshold slope) is the key factor to limit the operating supply voltage, and is given by [51],[55]

$$SS = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \underbrace{\frac{\partial V_G}{\partial \psi_S}}_{=m} \times \underbrace{\frac{\partial \psi_S}{\partial \log_{10} I_D}}_{=n} \tag{9}$$

The first term on the right-hand side of (9) is called the body factor ($m$), and the second term is the transport factor ($n$). The value of $SS$ would be significantly lowered by reducing either $m$ or $n$ or both. The transport factor for the planner and non-planner MOS devices cannot be lowered down below the $60mV/dec.$ at room temperature, due to the "*Boltzmann Tyranny*". However, the body factor is given by,

$$m = 1 + \frac{C_{Device}}{C_{ox}} \tag{10}$$

where $C_{Device}$ is the baseline capacitance of the device, and $C_{ox}$ is the overall oxide capacitance.

From (10), $m < 1$ can be feasible only when $C_{ox}$ has the negative value i.e., $C_{ox} < 0$. So, keeping this concept in mind, in 2008 S. Salahuddin et. al. proposed the concept of NC in conventional MOS devices by adding the FE



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layer into the gate stack. The FE layer within the gate stack as shown in Fig. 4, internally amplifies the voltage and preserves the device performance at a considerably low supply voltage. The working principle of NC-FET is like a conventional MOS device with added voltage amplification capabilities.

To understand the voltage amplification capability of FE material, consider the simple capacitance network of the MOS device as shown in Fig. 4. Herein, $C_{FE}$ is the induced capacitance in the FE layer, and connected in series with the oxide capacitance.

Applying the voltage divider rule, the amplification factor ($\beta$) can be expressed by [56]-[58],

$$\beta = \frac{\partial V_{int}}{V_G} = \frac{C_{FE}}{C_{FE} + C_{ox}} \tag{11}$$

From (11), due to the NC ($C_{FE} < 0$) provided by the FE layer, leads the $\beta > 1$.

The $SS$ of FET devices given in (9), can be expressed in terms of $\beta$, is given by

$$SS_{NC} = \left( \frac{\partial \log I_{DS}}{\partial V_G} \right)^{-1} = \frac{\partial V_{int}}{\partial \log I_{DS}} \times \frac{\partial V_G}{\partial V_{int}} = \frac{SS}{\beta} \tag{12}$$

In (12), $SS_{NC}$ is the subthreshold swing of NC-FET. Its value is always less than $SS$ of a conventional MOS device.

The overall applied voltage at gate terminal ($V_G$) is divided between FE layer voltage ($V_{FE}$) and surface potential ($\psi_S$). Mathematically given as [59],

$$V_G = V_{FE} + \psi_S \tag{13}$$

The overall channel charge density ($Q_{ch}$) in the channel region of NCFET is $Q_{ch} = C_{Device} \times \psi_S$. Fig. 5 (a) depicts the band diagram for NC-FETs when the $V_G$ is lower than the flat band voltage ($V_{FB}$), which will ensure the upward band bending near the oxide/semiconductor interface [60]-[62]. With the increase in $V_G$ the band near the oxide/semiconductor interface start bending downward as shown in Fig. 5(b). The field induced across the oxide layer makes the $\psi_S$ greater than the applied $V_G$ i.e. $\partial\psi_S/\partial V_G > 1$. This means that the $\psi_S$ is amplified against $V_G$. This amplification in $\psi_S$ also referred to as voltage amplification, will arrange more channel charges in the channel region.

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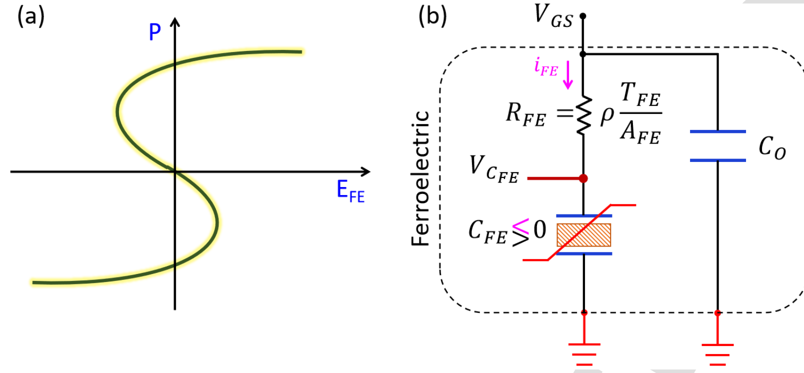


Figure 6: (a) The S-shaped curve of $P - E_{FE}$ in steady states exhibiting switching of polarization of FE materials. (b) Equivalent FE capacitor circuit for L-K model.

## 5. Modeling for NCFET

To develop the model for explaining the relation between polarization and voltage across FE materials several approaches have been discussed.

The total charge in ferroelectric materials ($Q_{FE}$) is given by [15]

$$Q_{FE} = A_{FE} \times (\epsilon_0 \times V_{FE}/T_{FE} + P) \tag{14}$$

where $\epsilon_0$ is vacuum permittivity, $V_{FE}$ is the voltage across the FE layer, $A_{FE}$ is an area of the FE layer, and $P$ is the polarization. The relation between $P$ and $V_{FE}$ has been modeled using several approaches. Two of which: 1) Landau-Khalatnikov (L-K) model, and 2) Miller model [42], are discussed below.

### *5.1. Landau-Khalatnikov (L-K) Model*

To formulate the $P - V_{GS}$ relation, the L-K model is the most straight forward approach, which is given as [63],[64],

$$-\frac{\partial U_{FE}}{\partial P} = \rho \frac{\partial P}{\partial t} \tag{15}$$

where $\rho$ is a damping parameter, representing the polarization lag during ferroelectric switching, and $U_{FE}$ is the energy density given in (6).

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An analytical model for transient negative capacitance is developed using a simplified circuit shown in Fig. 6(b), where a non-linear FE capacitor ($C_{FE}$) is connected in series with an intrinsic FE resistance ($R_{FE} = \rho \cdot T_{FE}/A_{FE}$) [65],[66].

Now, applying Kirchhoff's voltage law in Fig. 6(b), we have

$$V_{GS} = i_{FE} R_{FE} + V_{CFE} \tag{16}$$

here, term $i_{FE} = dQ_F/dt$ is the amount of current flowing through the $R_{FE}$.

The voltage drop across FE capacitor ($V_{CFE}$) is given as follows [15]:

$$V_{CFE} = T_{FE}\left(2\alpha P + 4\beta P^3 + 6\gamma P^5\right) \tag{17}$$

where symbols have their usual meanings.

Now, the (16) is given as

$$V_{GS} = \frac{dQ_F}{dt}\left(T_{FE}\frac{\rho}{A_{FE}}\right) + T_{FE}\left[2\alpha P + 4\beta P^3 + 6\beta P^5\right] \tag{18}$$

and putting $dQ_F \approx P \times A_{FE}$ in (18), we have

$$V_{FE} = \left(\rho\frac{T_{GS}}{A_{FE}}\right) \times \left(A_{FE}\frac{dP}{dt}\right) + T_{FE}\left[2\alpha P + 4\beta P^3 + 6\beta P^5\right] \tag{19}$$

In (19), the term $A_{FE}(dP/dt)$ is the displacement current, due to the polarization switching.

Rearranging the (19) as a rate of change of $P$ with respect to time ($t$), we have

$$\frac{dP}{dt} = \frac{V_{FE} - T_{FE}(2\alpha P + 4\beta P^3 + 6\gamma P^5)}{(T_{FE} \cdot \rho)} \tag{20}$$

From (20), it has been observed that $dP/dt$ is inversely proportional to the intrinsic ferroelectric resistance ($T_{FE} \cdot \rho$) [67].

The L-K theory dictates the voltage across the ferroelectric, which is given by (19). It is one of the most common techniques to model the voltage drop across the ferroelectric capacitor in NC-TEFT.

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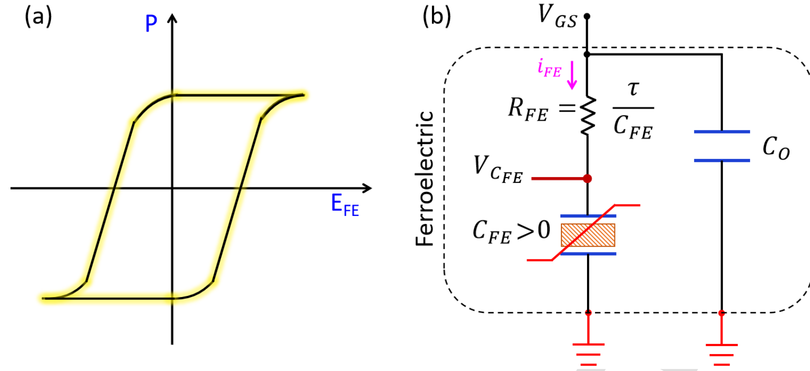


Figure 7: (a) Schematics of $P - E_{FE}$ curves in steady states with three different transitions of polarization switching. (b) Equivalent FE capacitor circuit for Miller model.

*5.2. Miller Model*

The Miller model is based on the concept of multidomain hysteresis shown in Fig. 7(a). However, Fig 7(b) shows the Miller model, having a series combination of $R_{FE}$ and $C_{FE}$ (like the L-K Model). Unlike the L-K model, in the Miller model the value of $C_{FE}$ is always positive. The $P - V_{GS}$ relation is given by [15],[68],[69]

$$P = P_S \left[ \tanh\left(\delta \times (V_{C_{FE}} \pm V_C)\right) + \frac{V_{CFE}}{V_P} \right] \tag{21}$$

where,

$$\delta = \frac{1}{V_C} \ln \frac{1 + P_R/P_S}{1 - P_R/P_S} \tag{22}$$

Here, $P_S$, $P_R$ are the saturation and remnant polarization respectively, $V_C$ is coercive voltage, and $V_P$ is the peak value of $V_{CFE}$.

The relation between $V_{CE}$ and $V_{CFE}$ is given by

$$\frac{dV_{CFE}}{dt} = \frac{1}{\tau} \left[ V_{GS} - V_{CFE} \right] \tag{23}$$

where, $\tau$ is the lag between $V_{GS}$ and polarization.

The key differences of discussed two models are summarized as follows [15],[16]:

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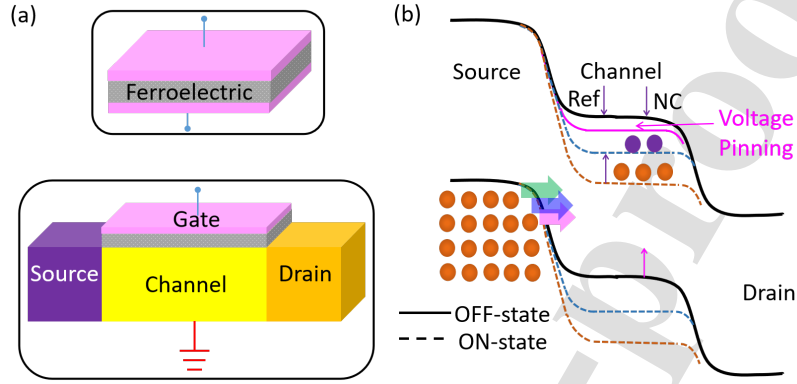


Figure 8: (a) 3D schematic view of top-gated NC-TFET. (b) Band diagram of n-type NC-TFET.

- Unlike the Miller model, the Landau model has the "S-curve" (shown in Fig. 6(a)) for the polarization versus electric field characteristics, which it cannot be able to capture the different states of polarization transitions due to which it will fail to portray the material properties of FEs.
- In the L-K model, $C_{FE}$ is inherently negative for a particular value of polarization, while in the Miller model, the $C_{FE}$ is always positive.
- In the L-K model, $R_{FE}$ is the elementary parameter and can be a function of the polarization field. It is not directly linked with $C_{FE}$ through the time constant parameter. Because for a negative value of $C_{FE}$, leads to negative $R_{FE}$, which is non-physical. Whereas in the Miller model, the time constant ($\tau$) is crucial, which is dependent on polarization and made $R_{FE}$ strongly dependent on $C_{FE}$.

## 6. Negative Capacitance Tunnel-FET

Note that the SS of conventional MOS devices is limited to $60mV/dec$ at room temperature, due to the Boltzmann distribution of electron energy. This



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is the fundamental obstacle to lowering the supply voltage and hence, the total power consumption. Therefore, the Tunnel FETs are proposed, in which the quantum mechanical BTBT is used to inject the charge into the channel, rather than the thermionic injection. However, it has been observed that achieving the sufficiently high drive $I_{ON}$ experimentally is extremely challenging for TFET devices. Therefore, the scientific community employs the concept of the negative capacitance of ferroelectrics in the TFET device as a performance booster.

The current conduction in Tunnel FET is based on the WKB transmission probability ($T_{WKB}$), which can be approximated as [70],[71]

$$T_{WKB} \approx exp\left(\frac{-\left(4\lambda\sqrt{2m^*}\sqrt{E_G^3}\right)}{3qh(E_G+\Delta\phi)}\right) \tag{24}$$

where $m^*$, $E_G$, and $\lambda$ are the effective mass, bandgap, and screening tunneling length. The $\lambda$ describes the spatial extent of the transition region at the source-channel interface [71].

In a TFET, keeping drain voltage constant, and increasing the gate voltage will inflect the surface potential. This will further increase the energy (difference between the conduction band of source, and valance band of drain) due to the reduction in the screening length. The subthreshold swing of a TFET can be calculated as [72]-[74] :

$$SS = \left(\frac{\partial V_G}{\partial(\log_{10} I_{DS})}\right) = \ln(10)\left[\frac{\partial V_{DS}}{V_D\ \partial V_G} + ((E+b)/E)^2\frac{\partial E}{\partial V_G}\right]^{-1} \tag{25}$$

where $V_D$ is the applied voltage at the drain terminal, $E$ is the electric field, and $b$ is a constant. From (25), it has been observed that the $SS$ of TFET is not a function of $k_BT/q$, i.e., not limited by the Boltzmann distribution.

In the NC-TFET, the NC concept is integrated into TFETs devices. The integration of two principles into a single device provides double advantages: 1): the lower $SS$ due to the NC effect and 2): the remarkably low leakage current. The preexisting polarization dipole of the FE layer discovers the concept of *voltage pinning* in NC-TFET as shown in Fig. 8(b). The charge carrier at the source-channel junction of TFETs in the ON state faces the triangular-shaped



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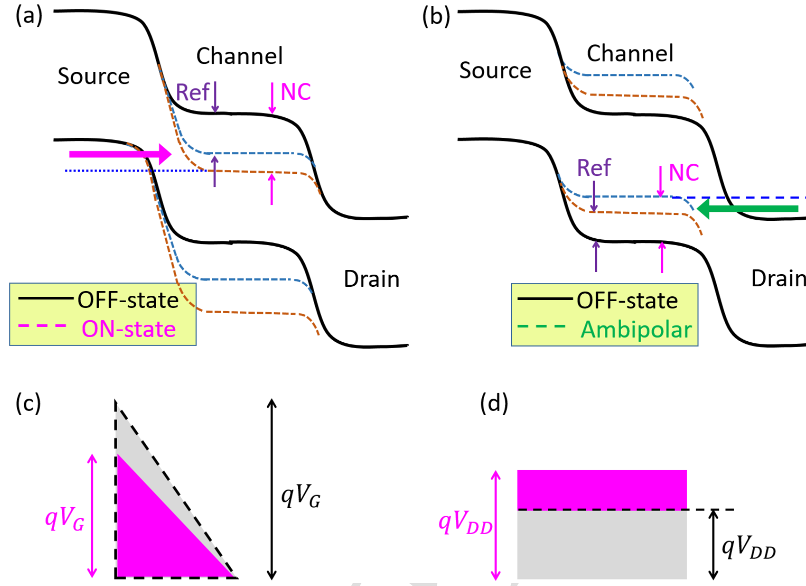


Figure 9: Band diagram of the NC-TFET which is presented for (a) $V_G > 0$ and (b) $V_G < 0$ for the normal and ambipolar conduction of the n-type NC-TFET. (c) Reduction in potential barrier presented at source/channel junction and, (d) increase in potential barrier presented at drain/channel junction of the n-type NC-TFET, due to voltage pinning.

potential barrier. It is reduced by reducing the energy difference between the valance band of the source region and the conduction band of the channel region. This will result in the enhancement in SS and $I_{ON}$ of the NC-TFET device. However, at the same time suppressing the ambipolar conduction by increasing the rectangular-shaped potential barrier at the drain-channel junction (shown in Fig. 9 (c) and (d) respectively) than the conventional TFET device [75],[76].

### *6.1. Voltage Pinning*

At the FE-metal interface in NC-TFET, the built-in voltage is formed due to the depolarization field. This built-in potential is attributed to the space charge at the interface. This effect in NC-TFET will further effectively reduce the $I_{OFF}$ by blocking the source tunneling when the device is in an OFF state.

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For the lower value of gate voltage ($V_G$), the internal voltage of NC-TFET is monopolized by the depolarization voltage ($V_{dipole}$, due to the FE dipole electric field). The surface potential ($\psi_S$) is given by [29],

$$\psi_S = \frac{C_{ox}}{C_{ox} + C_{Device}} \cdot V_{int} \tag{26}$$

From (26), for $C_{ox} \gg C_{Device}$, the $\psi_S$ is approximately equal to the $V_{int}$ (i.e., $\psi_S \approx V_{int}$). This means, that the $\psi_S$ is also pinned at a negative voltage value as shown in Fig. 10 (a).

With an increase in the gate voltage, from negative to positive value, the $\psi_S$ and $V_{int}$ will remain pinned at negative voltage value up to the certain value of externally applied gate voltage. This certain value of $V_G$ is used to overcome the depolarization field of FE materials. This effect is used to reduce the $I_{OFF}$ in NC-TFET, where the tunneling junction is highly sensitive to the transverse electric field which controls the reverse bias tunneling junction in sublet ways.

The relation between $V_G$ and $V_{int}$ is described considering the following regions of operation of NC-TFET: 1): voltage pinning region, where $V_{int}$ is quasi-constant, due to the polarization and the depolarization dipole field of the FE layer, and 2): the range of $V_G$ for completely depolarization (shown in Fig. 10(b)). This results in the following relationship [29]:

$$V_{int} = \frac{V_G}{1 + \frac{C_{ox} C_{Device}}{C_{ox} + C_{Device}} \times \frac{1}{C_{FE}}} \tag{27}$$

The stabilized NC region and a superior voltage amplification are observed at the possible lowest value denominator of (27).

## 7. Fabricated and Simulated NC-TFET Device Architectures

The first fabricated (to the best of our knowledge) NC-TFET is proposed by Lee et. al. in 2013, in which the FE layer is integrated into the gate stack by the lithography pattern and deposited by an electron-beam evaporator and lift-off process. The coupling FE layer in the gate stack is used to achieve the gate voltage and surface potential amplifications. Moreover, the integration of coupling the ferroelectric polarization is applied to hetro-tunnel FETs (HTFETs),

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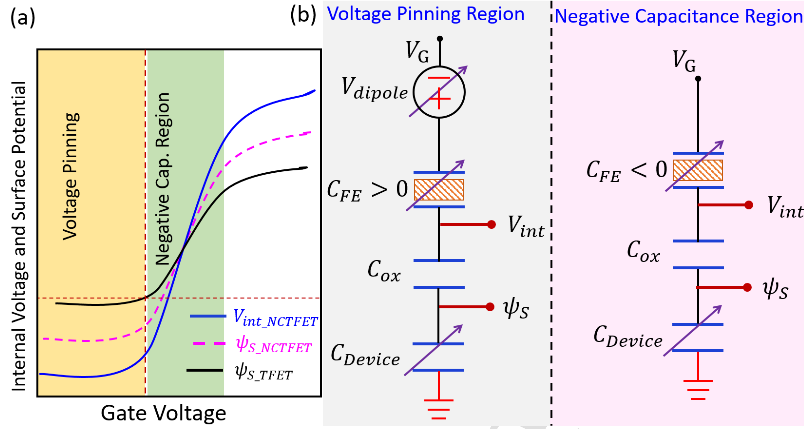


Figure 10: (a) Graphical representation of the internal voltage and surface potential of NC-TFET, (b) equivalent circuit for NC-TFET in voltage pinning and negative capacitance regions.

and nanowire (NW) TFETs [21]-[30]. The superior performance has been experimentally observed for the NC-TFETs, after FE layer deposition in the gate stack of the same TFETs device. Moreover, several theoretical investigations based on the device modeling and TCAD simulation have also been performed by several researchers.

The modeling and simulation of an ultra-thin body (UTB) double-gate (DG) NC-TFET (UTB-DG-NC-TFET), in which the FE layer is added in both the top and bottom gate stack has been investigated. The improved and non-hysteretic characteristics have been achieved by the proper optimization of top and bottom FE layer thickness, body thickness, and interfacial thickness [31]. Furthermore, the different nonplanner device architectures like gate all around (GAA) [32], T-shaped gate [33], and L-shaped gate [34], have also been investigated. Where the GAA is proposed for the superior gate electrostatics in the NC-TFET. However, the T-shaped gated NC-TFET has a lower threshold voltage and higher $I_{ON}/I_{OFF}$. This is because the T-shaped gate provides a larger tunneling area without changing the size of the devices. The NC vertical-

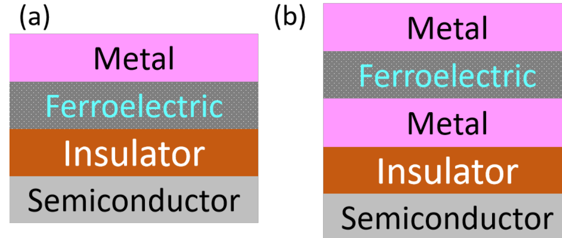


Figure 11: NC-TFET-based configurations structures (a) MFIS and, (b) MFMIS gate stack.

TFET is also used for negative-capacitance vertical-tunnel FET (NCVT-FET) to maximize its vertical tunneling over the corner tunneling. Negative capacitance enhances vertical tunneling more significantly than corner tunneling due to the amplified vertical electric field. A hybrid design that consists of an L-shaped gate and dual tunneling (DTD) TFET with a vertical FE gate insulator is proposed. The vertical FE layer will provide higher carrier tunneling from the source side to the channel region, while the L-patterned trench reduces the nonlinearity in the output characteristics. The higher BTBT rate at the source edge will cause the electric field crowding to be controlled by DTD [35]-[37]. Furthermore, the integration of the NC concept into the channel engineering, advanced channel materials-based TFETs like recessed channel NC-TFET (RC NC-TFET), and partial channel doping engineering have also been investigated with the help of TCAD simulation [38]-[41]. Some of the highly cited published work on NC-TFET to date have been summarized in Table I.

Finally, based on the experimental and theoretical research it has been concluded that the integration of the FE layer into the gate stack of planner and non-planner TFETs outperform in comparison to their TFET counterparts and will be a promising alternative candidate for future generation low power technology.

### *7.1. Gate Stack in NC-TFET*

During literature on NC-TFETs and NCFETs, two main gate stack architectures are used frequently: Metal–FE-Metal–Insulator–Semiconductor (MFMIS)

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and Metal-FE-Insulator-Semiconductor (MFIS) shown in Fig. 11(a), and (b) respectively. The major difference between these two architectures is the distribution of polarization along the channel. The additional internal gate in MFMIS ensures the uniform potential between the external and internal gate causing the constant FE polarization throughout the channel. It will amplify the surface potential in the entire channel region [77]. Unlike MFMIS, the MFIS has a nonuniform distribution of polarization along the channel region. In this case, the surface amplification takes place around the source region. The published literature ensures that the MFIS structure offers the lower SCEs, steep SS and high ON current at higher drain voltage in comparison to the MFMIS structure [78]-[83].

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Table 1: Comparison Among the Previously Reported NC-TFET Devices

| Year [Ref.] | Structure | FE Layer | SS (mV/dec.) | Highlights |
|---|---|---|---|---|
| 2013[21] | MFMIS | PZT | – | Experimentally demonstrated NC-TFET. |
| 2014[23] | MFMIS | PZT | – | Using FE layer in gate stack,to ensure steep SS. in tunnel field-effect transistors |
| 2016[31] | MFIS | PZT | ≈10 | Ultra-thin body double gate NC- tunnel FET (UTB-DG-NC-TFET). |
| 2017[32] | MFMIS | SBT | – | Mathematical demonstration of NC-GAA-TFET. gate stack is proposed. |
| 2018[26] | MFMIS | PZT | 20 | Strained silicon-nanowire based NC-TFET. |
| 2019[27] | MFIS | HZO | 54 | Experimental demonstration of NC-TFET |
| 2019[28] | MFIS | HZO | 44 | NC-TFET design based on junction depleted modulation. |
| 2020[34] | MFIS | Si:$HfO_2$ | 29 | L-patterned gate NC-TFET with highly doped dual tunnel diodes and vertical tunneling. |
| 2020[35] | MFMIS | HZO | 13.8 | The heterojunction NCVT-FET has been analyzed using TCAD to achieve lower $SS$ and $I_{OFF}$ |
| 2020[29] | MFMIS | PZT | 10 | Nanowire NC-TFET structure fabricated to ensure lower $SS$ and $I_{OFF}$. |
| 2021[22] | MFIS | – | 27 | A heterojunction NC-TFET has been designed. |
| 2021[38] | MFIS | $HfZrO_2$ | 43.9 | Partial channel doping is applied to mitigate the BTBT associated with the corner. |
| 2021[33] | MFIS | HZO | 18.32 | A T-shaped gate, Si based NC-TGTFET. |
| 2022[87] | MFMIS | HZO | 20.56 | GAA NCTFET, ensures larger $g_m$, and smaller $V_{Th}$ and DIBT. |



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## 8. Advantages of NCTFET: Device and Circuit Perspective

The FE layer causes the voltage amplification in NC-TFET, which will cause a better band bending and BTBT rate. Moreover, it will also reduce the $SS$ by reducing the body, and transport factors without any degradation in device performance. The lower $I_{OFF}$ and higher $I_{ON}$ current will certainly enhance the overall circuit performance, by adding the high switching speed at low supply voltage [84],[85].

### *8.0.1. Device Perspective: Negative Drain Induced Barrier Lowering (NDIBL)*

Unlike the conventional MOSFET, the increase in the drain to source voltage reduces the channel potential on NC-based MOS devices, resulting in negative drain-inducing barrier lowering (NDIBL). The NDIBL is used to reduce the scaling induced SCEs [43], [86], [87].

Combining the (16) and (17), we have the following equation,

$$V_{GS} = i_{FE}R_{FE} + T_{FE}(2\alpha P + 4\beta P^3 + 6\gamma P^5) \tag{28}$$

In the above equation $i_{FE}R_{FE} = V_{FE} = V_{int}$, and $P = Q_G - \epsilon_0 E \approx P$. So (26) is rewritten as

$$V_{int} = V_{GS} - T_{FE}(2\alpha Q_G + 4\beta Q_G^3 + 6\gamma Q_G^5) \tag{29}$$

As the NC-based MOS device enters into the NC region of operation, the $Q_G$ is lower than remnant polarization. Due to this phenomenon, the first term ($2\alpha Q_G$) in the bracket of (28) on the right-hand side has more dominance than the second and third terms. The $Q_G$ reduces with increase in $V_{DS}$, will lead to decrease in $V_{int}$, resulting the concept of NDIBL [88], [89].

The DIBL is the SCEs in the MOSFETs, and an identical concept known as drain-induced barrier thinning (DIBT) (also called DIBL in some literature) occurs in the TFET [90], [91]. The DIBT does not lower the potential barrier, it is thinning the potential barrier, and indicates the threshold voltage shift as a function of drain bias [92]. The DIBT in TFET arises due to the influence of the drain bias on the source-channel junction electric field and is more sensitive



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to the gate length of the TFET devices [93]-[95]. The DIBT is given by the equation

$$DIBT(or DIBL) = \frac{V_{Th,High} - V_{Th,Low}}{V_{DS,High} - V_{DS,Low}} \quad (30)$$

where $V_{Th,High}$, and $V_{Th,Low}$ are the threshold voltage at high and low value of $V_{DS}$. Fundamentally, the $V_{Th}$ is written as [94], [88]

$$V_{Th} = \phi_{MS} + 2\phi_{bi} + \frac{Q_G}{C_G} \quad (31)$$

In (31) $\phi_{MS}$ is the work function difference between metal and semiconductor, and $\phi_{bi}$ is the built-in potential. There are no influence on NC effect on $\phi_{MS}$ and $\phi_{bi}$. However, the $Q_G$, and overall gate capacitance ($C_G$) are severely affected by the NC effect, which can be better understood by the (29), and Fig. 4 respectively. Mazumdar et. al. [87] has been investigated the impact of the NC on GAA-TFET and ensured a lower DIBT than conventional TFET device. It has confirmed that the NC-based TFET devices may have higher speeds and lower power consumption.

*8.0.2. Switching Speed, Energy Efficiency and Defect Passivisation*

The FE capacitor requires the minimum time to provide voltage amplification [96]

$$\tau_{min} = \frac{CV_s}{I_{max}} = \frac{\rho_v t_{FE}}{2}\left(\frac{C_{Device}}{A}\right) \quad (32)$$

where $\rho_v$ is the viscosity coefficient which is less than $0.1\Omega m$, to achieve voltage amplification with a 1-ps rise time. For high-speed applications, it is necessary to find a suitable FE material with a relatively low $\rho$ (below $0.1\Omega m$) [96]. The concept of NC originates from the concept of the stored energy in the phase transition of FE materials. This provides the internal voltage amplification and improved energy efficiency for the NC-based TFET [97], [98]

The defect passivation plays an important role in reducing the depolarization field and trap-related leakage, and helps to achieve significantly high voltage amplification, and stabilizing multi-domain switching [99], [100].

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### 8.1. Analog Circuit Perspective

The transconductance ($G_{m,NC}$) of the NC-TFET device is an important parameter for analog circuit design, and affects the DC gain, bandwidth, transconductance efficiency, noise performance, etc. It is given by [26]

$$G_{m,NC} = \frac{\partial I_{DS}}{\partial V_G} = \frac{\partial I_{DS}}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial V_G} \quad (33)$$

or,

$$G_{m,NC} = g_m \times \beta \quad (34)$$

In (34), $g_m$ is transconductance of MOSFET device.

An analytical expression for the transconductance of the NC-TFET can be established (given in (34)) in terms of the product of transconductance and the amplification factor. The FE layer provides an effective negative capacitance, and $\beta > 1$, which boosted the overall transconductance of the NC-TFET devices.

The NC-TFET has higher $G_{m,NC}$ in comparison to the MOS devices. In general, the power dissipation ($P_D$) is related to the $G_{m,NC}$, is given by [85]

$$P_D = \frac{G_{m,NC}^2(|G_{m,NC}| + 2\kappa V_{Th})}{\kappa^2} \quad (35)$$

From (35), it has been concluded that the NC-TFET device with a higher value of $\kappa$, a lower value of $V_{Th}$ has a lower $P_D$ for constant $G_m$.

### 8.2. Digital Circuit Perspective

The voltage pinning effect occurs in the NC-TFET shown in Fig. 9(a). Due to it, the surface potential of NC-TFET is pinned to a higher negative value than the conventional TFET at the same gate voltage. It will further reduce $I_{OFF}$ and also suppress ambipolar conduction. The reduced $I_{OFF}$ in NC-TFET has significantly reduced power consumption in digital circuits.

The total power dissipation ($P_{Total}$) is given by [84]

$$P_{Total} = P_{static} + P_{dynamic} \quad (36)$$

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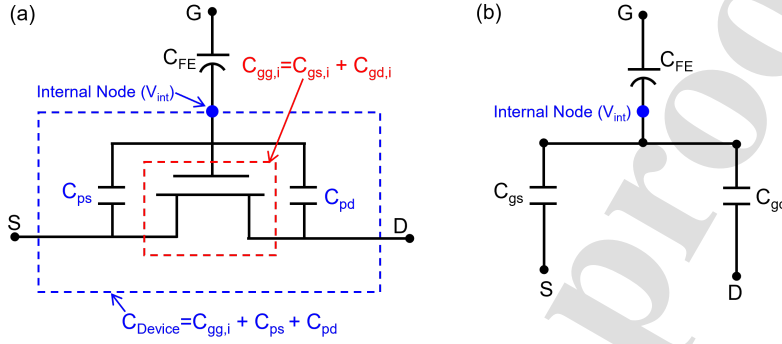


Figure 12: (a) Equivalent capacitance circuit model for the NCFET. (b) Gate and drain capacitance is responsible for the coupling between the drain node and internal node.

Here, $P_{static} = I_{OFF} \times V_{DD}$ is static power dissipation, and $P_{dynamic} = \alpha C_{Total} V_{DD}^2 f$ is the dynamic power dissipation, here $\alpha$ and $f$ is the number of bits switching and signal frequency respectively. The $I_{OFF}$ in NC-TFET is having a lower value than the conventional TFET. It will significantly reduce the $P_{static}$. While, the $P_{dynamic} \propto V_{DD}^2$, hence the $P_{dynamic}$ is reduced by effective scaling of $V_{DD}$.

## 9. Design Challenges

Despite having superior performance, the NC-TFETs have several limitations that create roadblocks for future endeavors. A few of them are listed as follows:

- The capacitance matching in NC-FETs is important to stabilize the device, which is maintained at a low range of gate voltage.
- The negative differential resistance (NDR) originated (in both planner and non-planner NC-based MOS devices) due to coupling between the drain voltage and internal voltage via a gate to drain capacitance ($C_{GD}$) [43], [86]. It leads to a decrease in the drain current of both types of devices. From Fig. 12 (b), the expression for the steady-state value of $V_{int}$, when

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the device is in the matched state (in negative capacitance region)[101]-[103]

$$dV_{int} = \frac{dV_{GS}}{1 - \frac{C_{GI}}{C_{FE}}} - \frac{dV_{GS}}{\frac{C_{C_{FE}-C_{GI}}}{C_{GD}}} = A_D dV_{GS} - \sum{}_D dV_{DS} \quad (37)$$

where, $C_{GI}$ is the positive gate capacitance belonging to the baseline transistor, which can be further split into the $C_{gs}$ and $C_{gs}$ shown in Fig. 12(b), $A_D$ is gain due to $FE > 1$, and $\sum_D$ is the drain-coupling factor.

The NDR can be optimized by the drain-coupling factor engineering ($\sum{}_D$) which is used to optimize the negative differential resistance in NC-based FET devices is formulated by using the Fig. 12(b) and given as follow [102],[103]

$$\sum{}_D = \frac{dV_{int}}{dV_{DS}} = \frac{C_{GD}}{C_{FE} + C_{Device}} \quad (38)$$

The $\sum{}_D$ depends on two key factors, first is the capacitance matching between the $C_{FE}$ and the device underlying capacitance ($C_{Device}$), and the second is the coupling capacitance formed between gate, and drain terminal ($C_{GD}$) [102].

- The heterostructure is formed at the metal/FE or FE/dielectric interface, which causes the fixed charge trapping at the interface. This is one of the most serious concerns faced by process engineers. The trapping and detrapping of interface charges will strongly affect the electrostatics inside the FE layer, and also creates defects at the grain boundary [104],[105].

- At gigahertz frequency, the NC-based FET may lose its advantages over the conventional FET, because the change in the polarization is quite small. This will result in the polarization term ($A_{FE} \times P$) in (14) being negligible, which provides the dynamic response to the overall charge in FE materials. So the $Q_{FE}$ is equal to the $A_{FE} \times (\epsilon_0 \times V_{FE}/T_{FE})$, and $C_{FE}$ behaves like linear capacitance, having a smaller value than the $C_{ox}$. This will further lead the voltage attenuation in NC-based devices [96].



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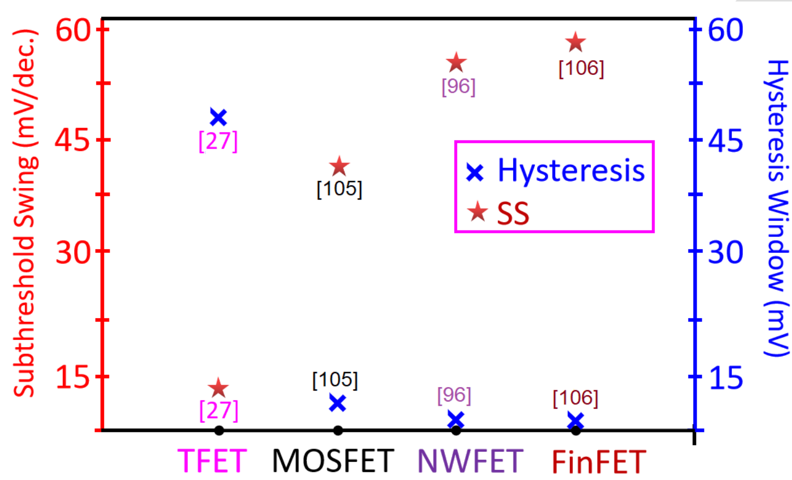


Figure 13: Performance comparison among the reported NC based NW-TFET, MOSFET, NWFET, FinFET devices.

- The large value of tunneling resistance at the source/channel junction will greatly reduce the tunneling probability of the charge carrier. As a result, the TFET is suffering from the low $I_{ON}$.

- Although the TFET process is compatible with conventional devices, due to the asymmetrical device design the sharing of the active area is difficult. This will affect the overall wafer area of the TFET-based device, which causes the TFET-based circuit to cost incompetent [106]. The optimization of the FE layer area, thickness, polarization, and coercivity must be scrutinized because these parameters have a major impact on the performance of NC-based FET devices [25], [107].

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Table 2: Comparison among the performance parameters of NCTFETs.

| Performance Parameter | Value |
|---|---|
| ON Currents ($I_{ON}$) | $135\mu A$ [87], $1.867mA$[109], $15\mu A$[116], $10mA$ [25] |
| ON-OFF Ratio ($I_{ON}/I_{OFF}$) | $10^{11}$ [87], $10^{10}$[109], $10^{7}$ [116], $10^{6}$ [25] |
| Subthreshold Swing ($mV/dec$) | 20.56[87], 10 [29], $>60$ [25], 39 [109] |
| Transconductance ($g_m$) (mS) | 7.87 |

## 10. Conclusion & Future Scope

This review paper presented the concept of NC in TFET based on the previous works that have been reported to date. Herein, we discussed how can a FE layer in the gate stack reduce the SS lower than the fundamental Boltzmann limit of $60mV/dec$. The NC-TFET has set a new boundary for the semiconductor industry and emerged as a potential substitute for conventional MOS devices. The performance of NC-TFET devices is compared in terms of better $I_{ON}/I_{OFF}$, and ultra-low leakage current. It is evident that NC-TFET has lower SS in comparison to the other NC-based conventional and non-planer MOS devices as shown in Fig. 13. A clear comparison among the NC-TFETs is listed in Table 2. The lower SS makes the NC-TFET-based device for the low-power integrated circuits (ICs). However, the optimized hysteresis window in NC-TFET verified the memory function of NC-TFET and makes it a potential candidate for the memories that should be emerging memory for NVM. Finally, in conclusion, the NC-TFET has the steepest SS among other devices, one can say that its SS is one of the closest to the ideal MOSFET device in terms of the SS at room temperature (shown in Fig. 14). The idea of Fig. 14 has been taken from the cover page of the IEEE Electron Device Letters [113].

The researchers must not confuse NC-FETs with ferroelectric FETs (FE-FETs). Although, both of them have identical gate stacks but have different

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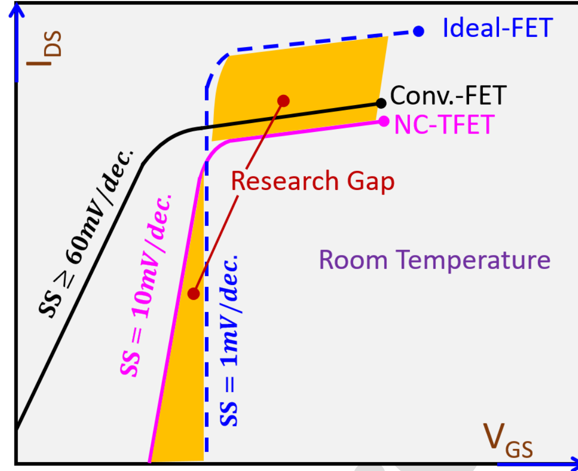


Figure 14: Comparison among the conventional FET, NC-TFET, and Ideal-FET.

functionalities. Unlike NC-FET, the FE-FET has hysteretic I-V characteristics (shown in Fig. 15) and has negative total gate capacitance. The total gate capacitance in NC-FET is positive, which means that the NC-FET is in the single stabilized stage.

To move forward with the research of NC-based transistors, the gap between the fundamentals of FE materials and transistors needs to be bridged. From Fig. 15 one can observe that PZT, SBZ, HZO, and Si: $HfO_2$-based FE materials are specially used in NC transistors and should enhance the performance in the future. Furthermore, to ensure better low power and steep SS and high drain current driving capability, several conventional and non-planer device architectures (like bulk NCFET, NC-FDSOI, NC-FinFET, NC-TFET, etc) physics are also researched by the different scientific communities. With these fascinating capabilities, the NC-TFET will fulfill the need for lower power, high-speed memories (FE already has NVM capabilities), digital circuits, neural networks, and neuromorphic computing [114]-[119].

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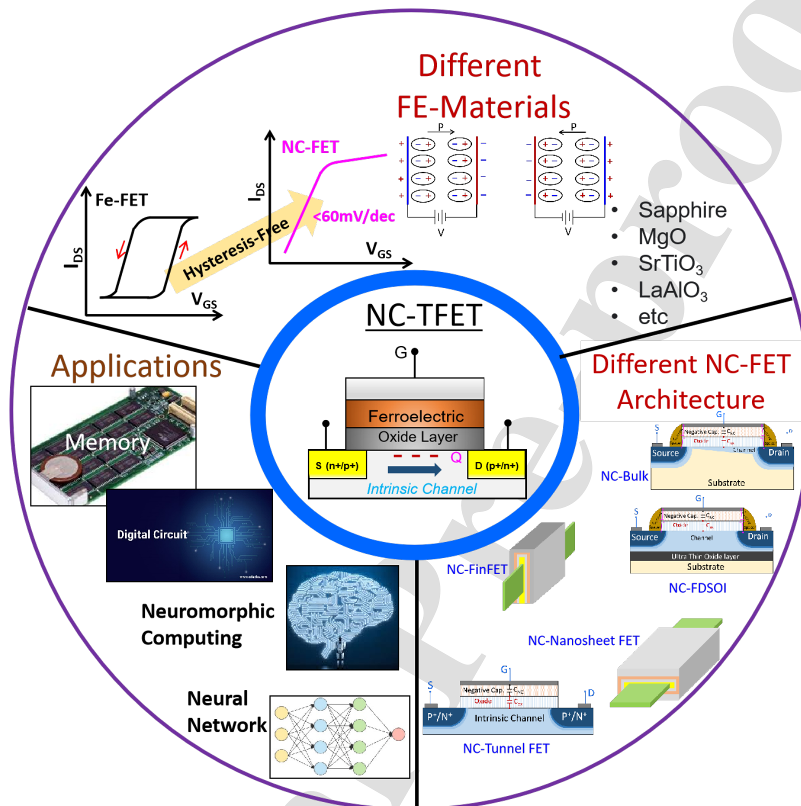


Figure 15: The Y-chart of NC-TFET to portray the future scope of the FE material to FET device to integrated system.

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## Authors Statements

Abhishek Kumar Upadhyay: Conceptualization, Methodology, Data curation, Writing-Original draft preparation. S.B. Rahi, S. Tayal, and Y. S. Song: Writing-Reviewing and Editing.

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**Declaration of interests**

☒ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

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