Thermal-Aware IC Chip Design by Combining High Thermal Conductivity Materials and GAA MOSFET

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***Abstract*—The high integration of integrated circuit (IC) chip design has made thermal-aware design as one of the first priorities of the modern IC chip industry. Even though the modern IC chip technologies have aimed to achieve thermal stability by optimizing circuit design, the rapidly growing integration requires thermal-aware design not only in circuit level but also in transistor level. Such thermal-aware design with bottom-up (from the transistor level to the packaging level) can be used to reliable IC chips. Moreover, since aluminum oxide (Al_2O_3, also known as alumina) is compatible with CMOS fabrication process and has excellent thermal conductivity, it is possible to efficiently accomplish the improved thermal-aware design. Specifically, Al_2O_3 has 59 times thermal conductivity compared to HfO_2, and 19 times thermal conductivity compared to SiO_2. In this paper, considering the outstanding thermal characteristics of Al_2O_3, we propose a comprehensive improvement including thermal characteristics by combining Al_2O_3 and GAA MOSFET. As a result, the maximum lattice temperature (T_{max}) in transistor has been significantly improved from 624 K to 518 K. In addition, capacitance of transistor could be also decreased, which will give benefits to inverter delay and three-stage ring oscillator (RO3) delay in IC chip.**

Keywords—Integrated Circuit (IC) Design; Thermal-aware Design; Thermal Characteristics; Thermal Conductivity; Low-Power Design; Aluminum Oxide

I. INTRODUCTION

With increasing integration of the Integrated Circuits (IC), thermal-aware design emerges as one of the first priorities of modern IC chip technology [1]. According to this demand, many researches have been broadly conducted for achieving thermal-efficient circuit design [2, 3]. However, even though this conventional approach with circuit optimization has successfully suppressed heat-generation, the novel IC chip made from sub-7 nm technology node requires more heat optimization [4-7]. Therefore, it has been widely accepted that IC chip needs to be thermally optimized not only in circuit level, but also in transistor level.

Unfortunately, most of transistor research has aimed to improve its own electrical characteristics, and the thermal characteristics has been not broadly researched [8-12]. This is because the improvement in thermal characteristics usually conflicts with improvement in electrical characteristics. For example, modern CMOS industry (such as *Intel*, *AMD*) plans to adopt gate-all-around (GAA) transistor structure for replacing FinFET structure and accomplishing low-power operation [13, 14]. However, since gate insulator (gate dielectric material) in GAA MOSFET completely wraps around silicon (Si) channel, the heat becomes hard to be dissipated.

This self-heating effect (SHE) not only degrades electrical characteristics, but also degrades several reliability issues in IC chip such as metallization lifetimes of circuit [15, 16], negative-bias temperature instability [17], hot-carrier induced degradation [18]. In this paper, for improving these concerns, novel GAA MOSFET structure is proposed by utilizing high thermal conductivity of Al_2O_3.

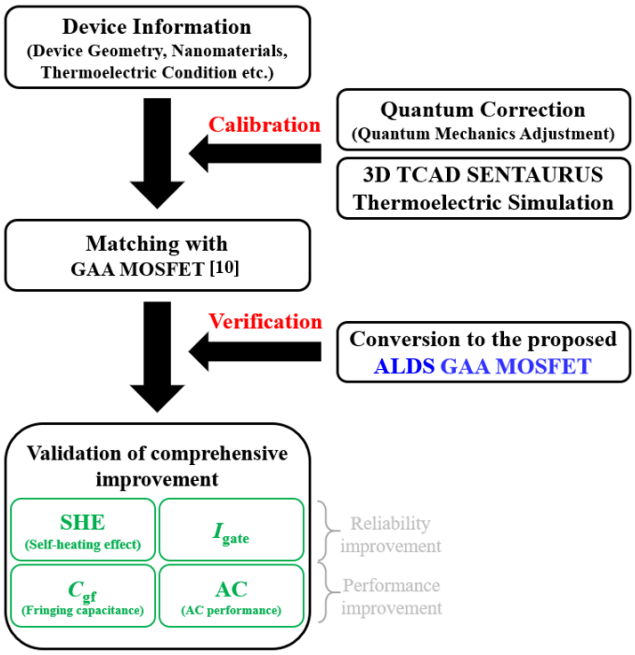

Figure 1. Overall workflow for validation of the proposed thermal-aware device design. From the proposed device structure, the thermal characteristics (SHE) and capacitance are simultaneously improved. Due to capacitance improvement, circuit performance such as RO3 delay, RC delay, inverter delay could be also improved.

II. Main Purpose of the Proposed Design Methodology

In our research, 2 main design goals are carefully adopted. First, for improving thermal performance of IC chips, thermal-aware design is adopted. Specifically, in designing transistor, the first goal is to suppress the increase of temperature during device operation.

Second, our research aims to improve the capacitance (C) of transistor. By doing so, our research tries to design low capacitance transistor for better circuit operation such as three-stage ring oscillator (RO3) delay, RC delay, and inverter delay.

III. Workflow and Calibration Process

Fig. 1 illustrates the overall workflow of this research. In order to reliably simulate the proposed structure with GAA MOSFET, the calibration of GAA MOSFET is carefully conducted and then the proposed Al_2O_3-based dual spacer (ALDS) structure is incorporated. Finally, the validation of the proposed ALDS GAA MOSFET is performed in terms of thermal characteristics and electrical characteristics.

During calibration, quantum correlations are carefully performed for I_{DS}-V_{GS} calibration under Synopsys Sentaurus™ 3D TCAD simulation tool [19]. Firstly, the electron mobility model (phumob/Enormal(Lombardi)/thin layer) is applied to consider interfacial surface calibration roughness scattering and Coulomb scattering. Then, quantum

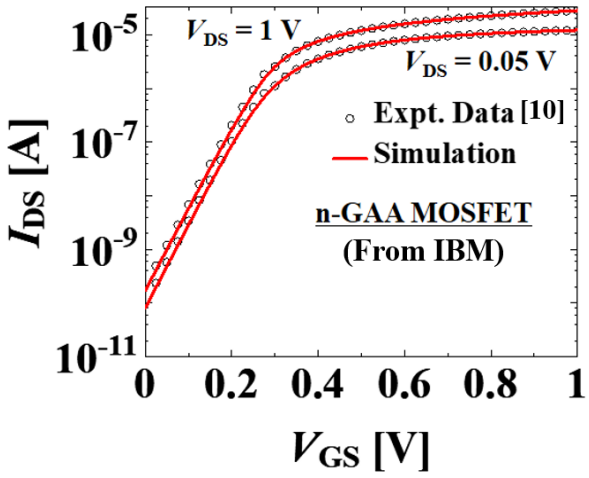

Figure 2. Calibration results with basic transfer characteristics (I_{DS}-V_{GS}). This figure shows that our simulation data is well fit with the real measured data [10].

model and velocity saturation model are applied, and gate work function (WF) is carefully adjusted. Finally, the thermal conductivity of nanomaterials, heat conduction paths, and thermal boundary condition (300 K) to each heat dissipation path are carefully applied for analyzing thermal characteristics.

As a result, Fig. 2 demonstrates that our simulation results are well fit with the measured data of GAA MOSFET [10, 11].

IV. Device Structure and Model Physics

A. Device Structure

For a fair comparison, the proposed ALDS GAA MOSFET [Fig. 3(a)] is compared with the previous dual spacer (DS) GAA MOSFET (HfO_2) [Fig. 3(b)] and the conventional GAA MOSFET (SiO_2) [Fig. 3(c)]. In the previous DS GAA MOSFET [Fig. 3(b)], P. K. Pal *et al.* intelligently utilized high-κ material (HfO_2) as inner spacer of DS, and SiO_2 as outer spacer of DS [12]. This previous DS structure was proposed for better inverter delay, and RO3 delay [12].

In designing all proposed structure, the 5-nm node technology values presented in the International Roadmap for Devices and Systems (IRDS) is carefully utilized ($L_{gate}/T_{Si}/T_{HfO2}/T_{SiO2}$ = 16/10/3/0.5 nm) [20].

In the proposed structure, Al_2O_3 is incorporated as inner spacer (see Fig. 3(a)) to improve thermal characteristics. In addition, the proposed ALDS GAA MOSFET structure is also designed to improve electrical characteristics as well. The lower permittivity of Al_2O_3 (compared to HfO_2) improves alternating current (AC) performance and fringing capacitance (C_{gf}), which will enhance circuit performance as well. In essence, our design methodology utilizes the high thermal conductivity and low permittivity of Al_2O_3.

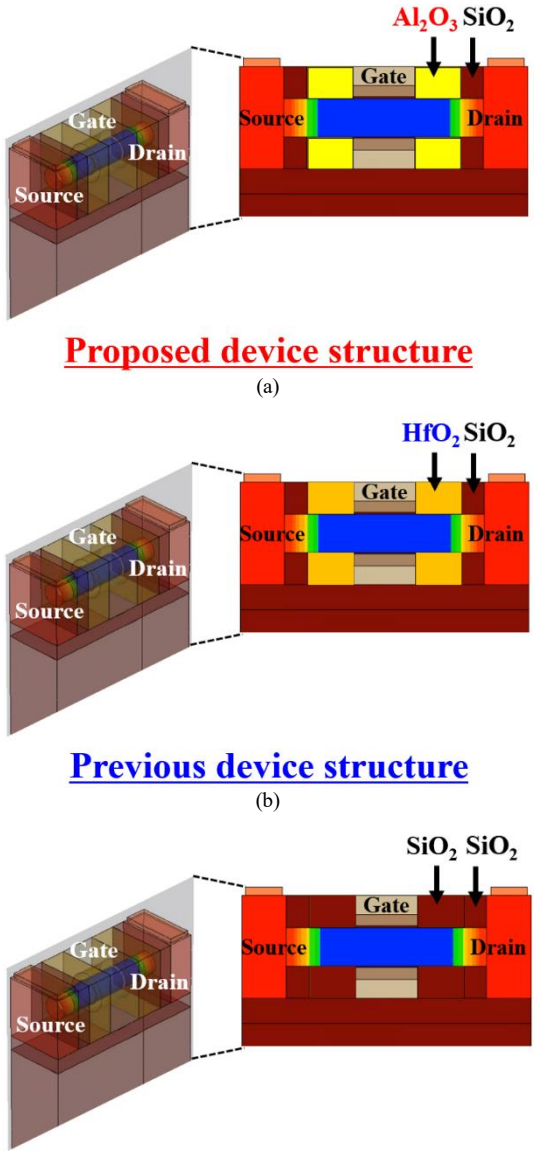

Figure 3. Schematic diagram of (a) the proposed device structure, (b) previous device structure, (c) conventional device structure. The proposed ALDS GAA MOSFET features dual spacer incorporating Al_2O_3 for thermal improvement and AC performance improvement.

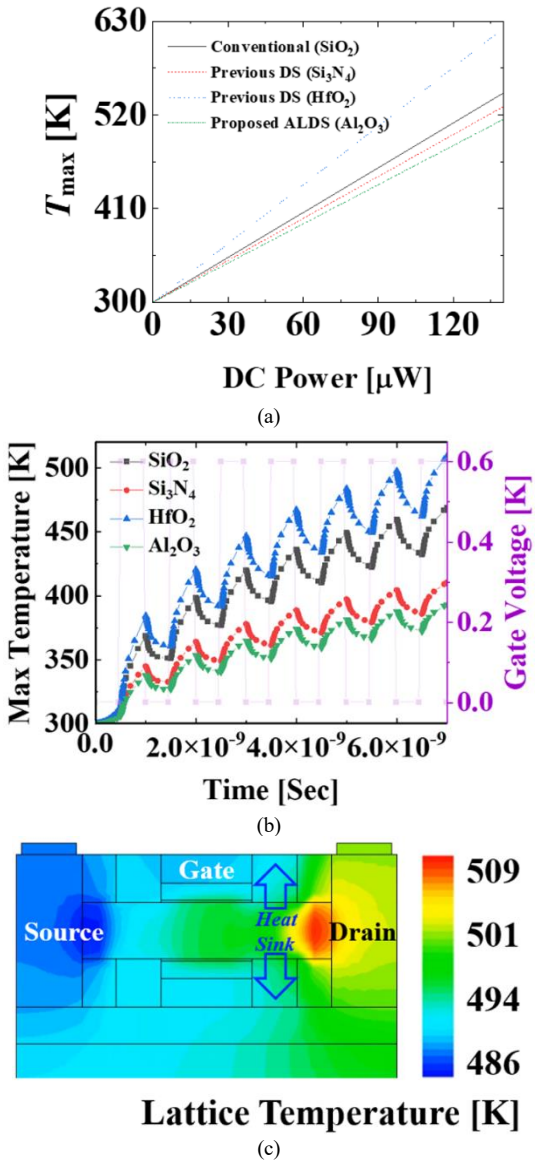

Figure 4. (a) Maximum temperature comparison with respect to DC power, (b) AC performance comparison with four different materials, (c) Cross-sectional view describing the location of heat sink and lattice temperature. Since the Al_2O_3 in the proposed structure acts as effective heat sink, maximum temperature could be significantly improved.

V. Simulation Results and Discussion

A. Improvement of Thermal Performance by the Proposed ALDS GAA MOSFET

Fig. 4 explains thermal characteristics in four different structures. Regarding maximum temperature (T_{max}), the proposed ALDS GAA MOSFET shows best SHE due to the excellent thermal conductivity of Al_2O_3 [Fig. 4(a)]. This thermal improvement also found in AC operation [Fig. 4(b)], since Al_2O_3 in the proposed ALDS GAA MOSFET acts as effective heat sink [Fig. 4(c)].

B. Model Physics for Investigating Thermal and Electrical Characteristics

To investigate the thermal and electrical characteristics, several quantum mechanics model such as Shockley-Read-Hall (SRH) recombination, high field saturation, Fermi, and thermodynamic models are applied. In addition, Fowler Nordheim (FN) tunneling, trap-assisted-tunneling (TAT), and direct tunneling models are also considered for carefully investigating the electrical characteristics.

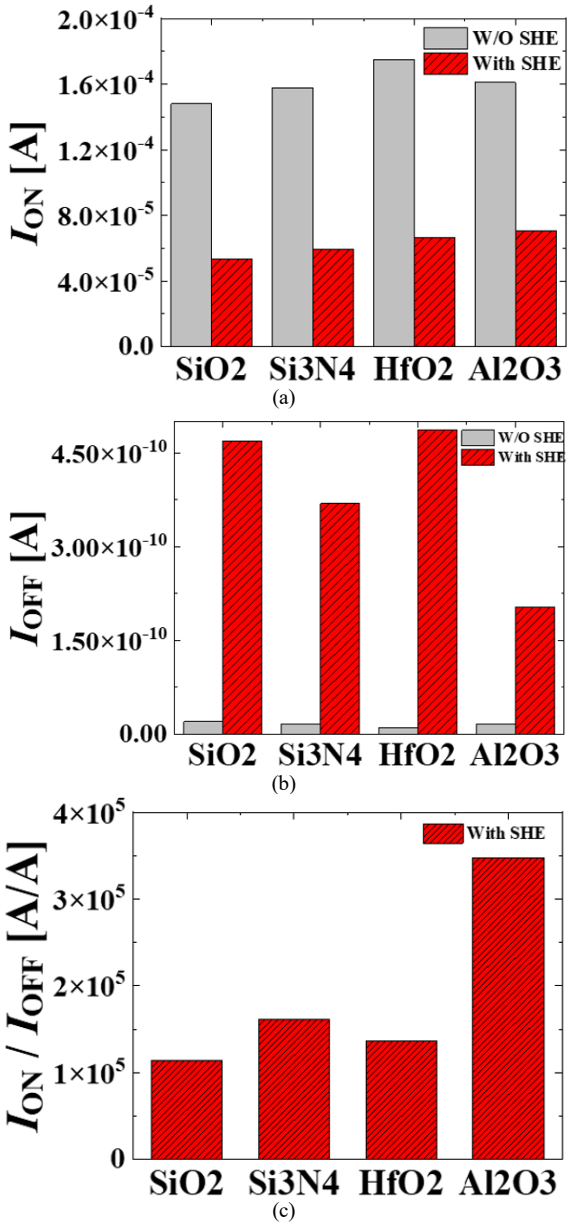

Figure 5. Comparative analysis between four different spacer structures under ideal condition (W/O SHE) and real condition (With SHE), in terms of (a) on-current (V_{GS} = V_{DS} = 0.6 V), (b) off-current (V_{GS} = 0 V, V_{DS} = 0.6 V), and (c) on-off current ratio. Since the proposed structure has lowest increase of temperature during operation, it has highest electron mobility and highest on-current.

B. *Improvement of On-current and Off-current by the Proposed ALDS GAA MOSFET*

Fig. 5 illustrates the on-current (I_{on}) comparison under ideal condition (W/O SHE) and real condition (with SHE). Under ideal condition (W/O SHE), the previous DS GAA MOSFET (HfO_2) shows the best I_{on}, since HfO_2 has the highest permittivity (permittivity of $SiO_2/Si_3N_4/HfO_2/Al_2O_3$ = $3.9\varepsilon_0/7.5\varepsilon_0/22\varepsilon_0/8.9\varepsilon_0$). However, under real condition (with SHE), our proposed ALDS GAA MOSFET shows best I_{on}, and then the previous DS GAA MOSFET (HfO_2) follows [Fig. 5(a)]. This can be explained by the degradation of electron mobility due to temperature increase. Specifically, the previous DS GAA MOSFET (HfO_2) has worst T_{max} due to the lowest thermal conductivity of HfO_2 [Fig. 4], and mobility degradation from SHE causes significant decrease of I_{on} in the previous DS GAA MOSFET (HfO_2) [Fig. 5(a)]. On the other hand, the conventional GAA MOSFET (SiO_2) shows the worst I_{on} performance, which means it is hard to be adopted to the next generation IC chips.

Regarding off-current (I_{off}), the previous DS GAA MOSFET (HfO_2) shows highest I_{off} [Fig. 5(b)], since the SHE causes the increase of I_{off} due to increased energy of free electrons. As a result, the proposed ALDS GAA MOSFET shows best on-off current ratio (I_{on}/I_{off}) [Fig. 5(c)].

C. *Improvement of Capacitance by the Proposed ALDS GAA MOSFET*

In addition, as illustrated in Fig. 6, the proposed ALDS GAA MOSFET also has better fringing capacitance (C_{gf}), compared to the previous DS GAA MOSFET (HfO_2). This is because the Al_2O_3 has permittivity of $8.9\varepsilon_0$, which is smaller than the permittivity of HfO_2 ($22\varepsilon_0$). Therefore, when the proposed ALDS GAA MOSFET is adopted, the circuit performance (such as RO3 delay, RC delay, inverter delay) is also possible to be improved.

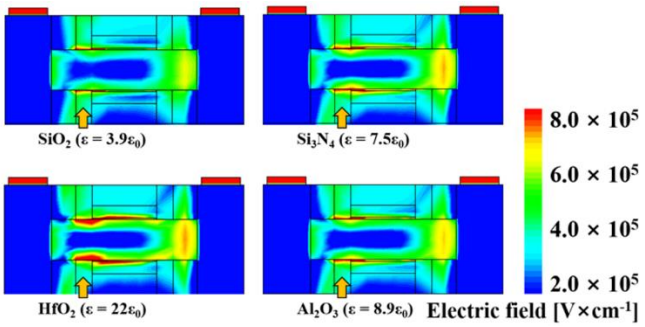

Figure 6. Distribution of electric field for comparing the fringing capacitance. Since Al_2O_3 has lower permittivity compared to HfO_2, the proposed structure has better C_{gf} compared to the previous structure with HfO_2. Therefore, our structure is expected to show better RO3 delay, RC delay, and inverter delay.

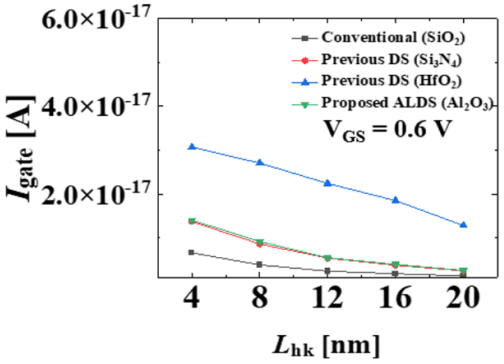

Figure 7. Gate current improvement achieved by the proposed structure (L_{hk} stands for length of inner spacer). Compared to the previous DS structure (HfO_2), our device structure shows better gate current characteristics.

D. Improvement of Gate Current by the Proposed ALDS GAA MOSFET

If gate current (I_{gate}) increases, the transistor's reliability becomes worse. This is because the gate current through gate insulator (gate dielectric oxide) deteriorates insulator quality and insulator will no longer properly act as insulator. This leads to fast failure in IC chips. Therefore, it is desirable to suppress I_{gate} as much as possible.

As demonstrated in Fig. 7, the proposed ALDS GAA MOSFET also has better I_{gate} characteristic, compared to the previous DS GAA MOSFET (HfO_2). This is because the Al_2O_3 has bandgap of 7.0 eV, which is greater than bandgap of HfO_2 (5.8 eV). Therefore, undesirable I_{gate}, which degrades reliability of transistor and circuit, could be also suppressed by the proposed ALDS GAA MOSFET.

Namely, comprehensive improvement of four characteristics (T_{max}, AC performance, C_{gf}, I_{gate}) could be achieved by the proposed ALDS GAA MOSFET. In essence, our proposed structure utilizes the advantage of high thermal conductivity, low permittivity, high bandgap of Al_2O_3.

E. Plans for Future Research

This paper has demonstrated electrical/thermal performances improvement, especially in transistor level. According to the result shown in this research, it is quite expected that our proposed design technique will be also possible to improve circuit performance. In accordance with this expectation, our research group is going to expand our field of research on circuit level. Especially, we are going to research improvement of gain in CMOS amplifier achieved by the improvement of transistor performance. In addition, more in-depth research will be also conducted to specifically investigate the effect of spacer length (L_{HfO2}) on transistor performance and circuit performance. Our research group would like to show appreciation to the reviewers of 2022 International Conference on Circuits, Systems and Simulation (ICCSS) for their times and efforts to generously review this manuscript. In addition, the authors are deeply appreciated in advance the times and efforts that the anonymous referee of IEEE Transactions on Electron Devices (IEEE TED) will generously share for reviewing our future research.

VI. Conclusion

In order to effectively perform thermal-aware design in IC chips, we designed thermally efficient transistor. Due to the excellent thermal conductivity of aluminum oxide (Al_2O_3, alumina), the maximum temperature (T_{max}) has been significantly decreased from 624 K to 518 K. In addition, our transistor also has additional advantages in terms of capacitance (C), which will enable improvement in three-stage ring oscillator (RO3) delay and inverter delay in up-coming IC chips. In essential, our proposed structure utilizes the high thermal conductivity, low permittivity, and high bandgap of Al_2O_3. Our proposed structure is very strategic for the future scaling IC chip technology with improved device reliability.

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