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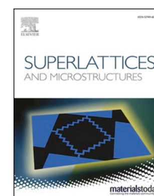

Performance evaluation of gate engineered InAs–Si heterojunction surrounding gate TFET

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ABSTRACT

In semiconductor industry, at nanoscale dimensions, numerous field effect devices have been proposed and investigated for further improvement in performance of low power circuit and system. In the present research report, a novel low power FET device structure namely: Surrounding Gate Triple Material Heterojunction Tunnel Field Effect Transistor (SGTM-heTFET) has been proposed with the analytical modeling approach. The benefits of surrounding gate and tunnel FETs are coupled to create a new structure, to decrease short channel effects. Three different gate materials with different work functions replace the gate material that surrounds the device. An analytical model of surface potential(ψ), electric field(E) and drain current (I_{DS}) have been developed for SGTM-heTFET. With the use of low work function material such as 4.0eV, 4.6eV and 4.0eV, the proposed model shows a better ON current of 10^{-5} A/μm for a V_{GS} of 0.7V, ON-OFF ratio of 10^{10} with the sub-threshold swing of 50mV/dec. The developed model's for SGTM-heTFET shows excellent device characteristics and have been verified using TCAD simulation, ensuring the model's accuracy.

1. Introduction

CMOS devices are scaled down to nanometre technology, in order to obtain low power consumption and noise immunity. Scaling down, the devices in an assertive manner not only reduces the power but also offers more packaging density and switching speed. This makes the device to suite for high frequency applications [1–4]. However, the limitations experienced are increase in short channel effects and degradation in the device performance. The degradation is caused not only because of the short channel effect but also due to the increase in subthreshold swing than fundamental limit in the MOSFET. It raises above 60 mV/decade and increases the leakage current (OFF current) [4–6]. One of the promising devices that offers low power application is Tunnel FET (TFET), which works under reverse bias condition and has a p-i-n (p-type; intrinsic; n-type) structure. TFET works on the principle of injecting the majority carrier through the source region by which it reaches the channel by band-to-band tunnelling mechanism. This makes the subthreshold swing to limit its value to 60 mV/decade. However, the major limitation of TFET is the ON current. Due to this low ON current the performance of the device gets affected. In order to overcome the drawbacks, various device architectures like dual gate, triple gate, GAA, surrounding gate and quadruple gate architectures are proposed [7–11] and various device geometry modifications also caried out

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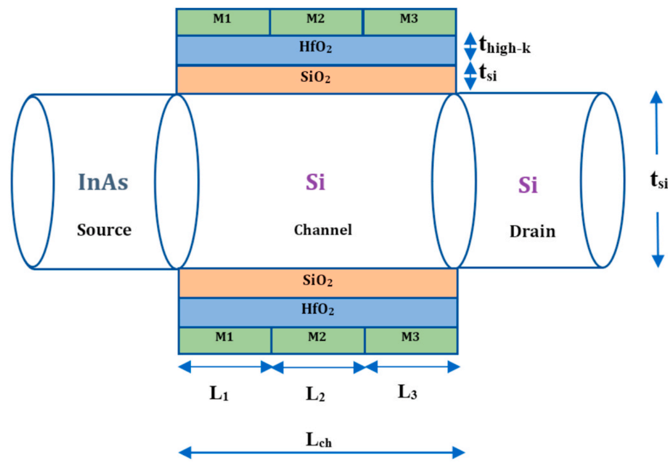

Fig. 1. Structure of surrounding gate triple material heterojunction TFET.

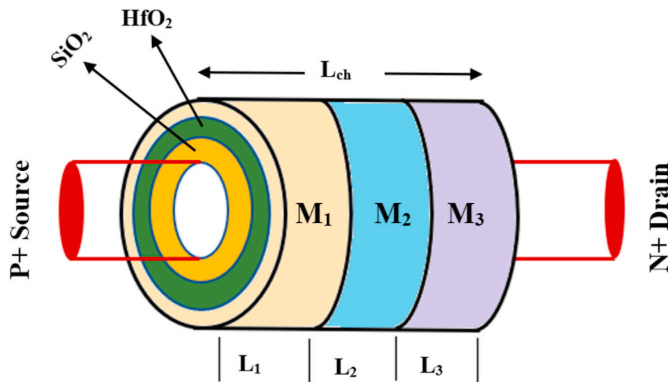

Fig. 2. 3D view of Surrounding Gate Triple Material Heterojunction TFET.

Table 1
Device parameters.

Parameters	Value
Doping at Source	$1x10^{20}$ cm^{-3}
Doping at Channel	$1x10^{17}$ cm^{-3}
Doping at Drain	$5x10^{18}$ cm^{-3}
Silicon Body thickness (t_{si})	20 nm
Oxide layer thickness(t_{ox})	1 nm
High-k material thickness($t_{high\text{-}k}$)	1 nm
Channel length (L_{ch})	45 nm
Metal work function (φ_{M1}, φ_{M2}, φ_{M3}) (Al, Mo, Sb)	4.0–4.7eV
Metal Gate Lengths (L_1, L_2, L_3)	15 nm, 15 nm, 15 nm

[12–19]. This lowering of subthreshold swing regime makes the improvement in device performance and also reduces the static power consumption.

2. Device structure and simulation model

In this work, heterojunction arrangement namely, Indium Arsenide (InAs) –Si with triple material and surrounding gate geometry are merged to form a new structure. InAs exhibits thin bandgap and high mobility taken as source material and Silicon material is used in channel and drain region. The probability of the tunnelling & drain current is enhanced by reducing the tunnelling barrier width between source-channel by which band bending occurs and this is made possible by the introduction InAs material. Here, to decrease the leakage current through gate oxide layer, high-k dielectric (Hafnium oxide) oxides are used and also to minimize the scattering due

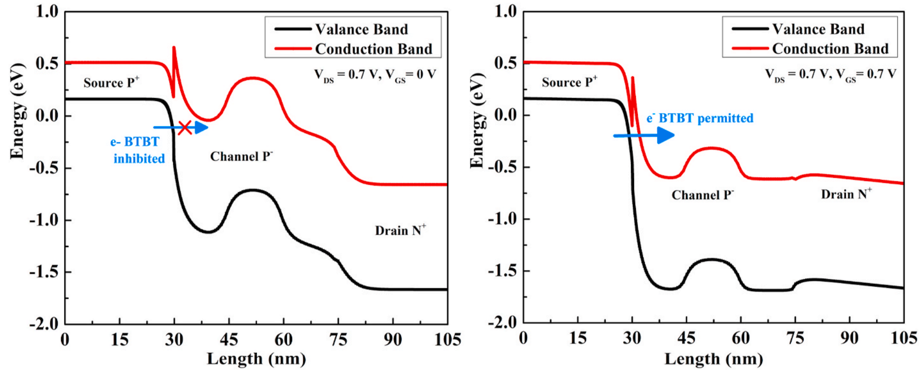

Fig. 3. Energy band diagram of SGTM-heTFET for OFF & ON State.

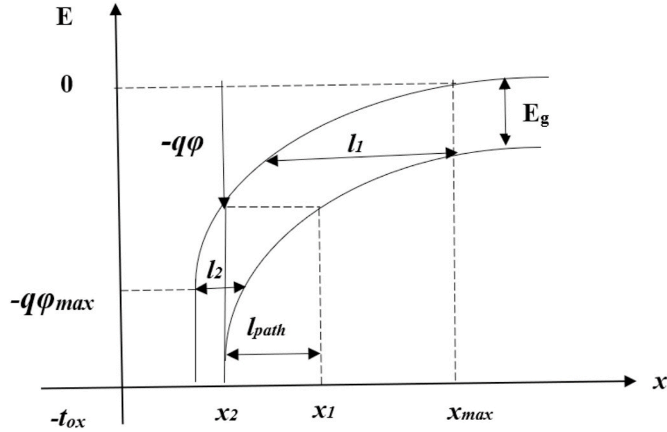

Fig. 4. Energy band diagram and minimum tunneling path of SGTM-heTFET.

to phonons, to increase the carrier mobility an intermediate layer with SiO_2 has been placed between the silicon channel and high-k dielectric. Fig. 1 depicts the proposed device structure of SGTM-heTFET and Fig. 2 gives the 3-D view of the proposed device. The proposed device structure is simulated using TCAD simulation tool and the several device parameters used in the simulation is given in Table 1.

The band diagram of the proposed device structure is given in Fig. 3a and b which depicts the band diagrams in ON and OFF state. The existence of large potential barrier between the source and channel during the OFF state resulted in no tunneling. As the gate voltage surpasses the threshold voltage, the potential barrier becomes narrower which in turn allows notable amount of tunneling current (see Fig. 4).

3. Analytical model

3.1. Surface potential model

The Poisson equation in cylindrical coordinates is given as follows

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi(r,z)}{\partial r}\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=-\frac{qN_C}{\varepsilon_{si}} \tag{1}$$

for. $0 \le z \le L$, $0 \le r \le R$

where, φ(r,z) – represents the 2D potential profile.

N_C – channel doping
ε_{si} – silicon permittivity
R – radius of silicon nanowire

➢ Using Young's approximation

$$\varphi_i(r,z) = f_{0i}(z) + f_{1i}(z)\, r + f_{2i}(z) r^2 \tag{2}$$

Where $f_{0i}(r,z)$, $f_{1i}(z)$, $f_{2i}(z)$ are used as Z functions and i = 1,2,3.

Region 1: $0 \le z \le L_1$

$$\varphi_1(r,z) = f_{01}(z) + f_{11}(z)\, r + f_{21}(z) r^2 \tag{3}$$

Region 2: $L_1 \le z \le L_2$

$$\varphi_2(r,z) = f_{02}(z) + f_{12}(z)\, r + f_{22}(z) r^2 \tag{4}$$

Region 1: $L_2 \le z \le L_3$

$$\varphi_3(r,z) = f_{03}(z) + f_{13}(z)\, r + f_{23}(z) r^2 \tag{5}$$

The Poisson equation is solved by using necessary boundary condition, resulting in a potential profile.

1. The value of electric field is zero at the Centre for silicon, therefore

$$\left.\frac{d\varphi(r,z)}{dr}\right|_{r=0} \tag{6}$$

$\varphi(0,z) = \varphi_C(z)$ this will give.
$f_{11}(z) = f_{12}(z) = f_{13}(z) = 0$, where $\varphi_C(z)$ represents center potential.

2. Surface potential is derived from equations (3)–(5) and calculated by replacing the variables r as R, thus generally written as,

$$\varphi_i(r,z) = \varphi_{Ci}(z) + f_{2i}(z)\, r^2\,, \quad \mathrm{i} = 1, 2, 3 \tag{7}$$

3. The electric field at the silicon and the dielectric interface can be written as

$$\left.\frac{d\varphi_1(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS1} - \varphi_{S1}(z)}{t'_{oxeq}} \tag{8}$$

$$\left.\frac{d\varphi_2(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS2} - \varphi_{S2}(z)}{t'_{oxeq}} \tag{9}$$

$$\left.\frac{d\varphi_3(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS3} - \varphi_{S3}(z)}{t'_{oxeq}} \tag{10}$$

Where $t'_{oxeq} = t_{ox} + \frac{\varepsilon_{ox}}{t_{\acute{o}x}} [t_{high-k} + t_{ox}]$

$t_{\acute{o}x} - SiO_2$ *thickness*

$t_{ox} - HfO_2$ *thickness*

ε_{ox} – *Permittivity of* SiO_2

Using the above boundary conditions, the value of center potential can be obtained as

$$\varphi_{C1}(z) = \varphi_{S1}(z)\left[1 + \frac{\varepsilon_{ox}}{2\varepsilon_{si}} \frac{V_{GS1}}{t'_{oxeq}} R\right] - \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS1}}{t'_{oxeq}} R\,; \quad 0 \le z \le L_1 \tag{11}$$

$$\varphi_{C2}(z) = \varphi_{S2}(z)\left[1 + \frac{\varepsilon_{ox}}{2\varepsilon_{si}} \frac{V_{GS2}}{t'_{oxeq}} R\right] - \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS2}}{t'_{oxeq}} R\,; \quad L_1 \le z \le L_2 \tag{12}$$

$$\varphi_{C3}(z) = \varphi_{S3}(z)\left[1 + \frac{\varepsilon_{ox}}{2\varepsilon_{si}} \frac{V_{GS3}}{t'_{oxeq}} R\right] - \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{GS3}}{t'_{oxeq}} R\,; \; L_2 \le z \le L_3 \tag{13}$$

The above equations represent the center potential at three different material regions. Substituting equations (7)–(11) in the given Poisson equation in (1) and after simplification,

$$\frac{2}{R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{GS1}-\varphi_{S2}(z)}{t'_{oxeq}}+\frac{d^2\varphi_{C1}(z)}{dz^2}-\frac{d^2\varphi_{S1}(z)}{dz^2}\left[-\frac{r^2}{2R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{t'_{oxeq}}\right]=-\frac{qN_C}{\varepsilon_{si}} \tag{14}$$

$$-\frac{2}{R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\varphi_{S2}(z)}{t'_{oxeq}}-\frac{d^2\varphi_{S1}(z)}{dz^2}\left[-\frac{r^2}{2R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{t'_{oxeq}}\right]=-\frac{qN_C}{\varepsilon_{si}}-\frac{2}{R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{GS1}}{t'_{oxeq}}-\frac{d^2\varphi_{C1}(z)}{dz^2} \tag{15}$$

Let. $\lambda^2=\left(\frac{R}{2}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)t'_{oxeq}\alpha=\frac{1}{\lambda^2}$ and $\beta_i=-\frac{qN_C}{\varepsilon_{si}}-\frac{V_{GS}}{\lambda^2}$ therefore equation (15) becomes

$$-\alpha\varphi_{S1}(z)-\frac{d^2\varphi_{S1}(z)}{dz^2}\left[-\frac{r^2}{2R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{t'_{oxeq}}\right]=\beta_i-\frac{d^2\varphi_{C1}(z)}{dz^2} \tag{16}$$

After rearranging the above expression with necessary substitutions, equation (16) can be expressed as

$$\frac{d^2\varphi_{S1}(z)}{dz^2}-\alpha\varphi_{S1}(z)=\beta_i \tag{17}$$

The common solution for equation (17) can be written as

$$\varphi_{Si}(z)=Ne^{\sqrt{\alpha}z}+Oe^{-\sqrt{\alpha}z}-\frac{\beta_i}{\alpha} \tag{18}$$

Equation (18) can be expressed as following to obtain surface potential expression for i = 1,2,3 and

$$\varphi_{S1}(z)=Ne^{\sqrt{\alpha}z}+Oe^{-\sqrt{\alpha}z}-\frac{\beta_1}{\alpha}\ ;\ 0\le z\le L_1\ under\ M_1 \tag{19}$$

$$\varphi_{S2}(z)=Ue^{\sqrt{\alpha}(z-L_1)}+Ve^{-\sqrt{\alpha}(z-L_1)}-\frac{\beta_2}{\alpha}\ ;\ L_1\le z\le(L_1+L_2)\ under\ M_2 \tag{20}$$

$$\varphi_{S3}(z)=Je^{\sqrt{\alpha}(z-L_1-L_2)}+Ke^{-\sqrt{\alpha}(z-L_1-L_2)}-\frac{\beta_3}{\alpha}\ ;\ (L_1+L_2)\le z\le L\ under\ M_3 \tag{21}$$

where N,O,U,V,J,K are arbitrary constants and the following boundary conditions are taken into consideration to solve for the constants respectively.

At source side, heterojunction is formed since the source is made up of InAs and the channel is made up of Si and the potential is given as $\varphi(r,0) = V_{bi}(S)$, where

$$V_{bi}(s)=\frac{1}{q}\left\{[\chi_1-\chi_2]+0.5[E_{g1}-E_{g2}]+qV_T ln\frac{N_V}{N_i}\right\} \tag{22}$$

χ_1 – *electron affinity of InAs*

χ_2 – *electron affinity of Si*

At drain side, since both the channel and drain are made up of Si, the potential is given as.
$\varphi(r,L) = V_{bi}(D)+V_{DS}$, where

$$V_{bi}(D)=\left(\frac{kT}{q}\right)ln\left(\frac{N_DN_C}{{n_i}^2}\right) \tag{23}$$

Surface potential at the edge of two different metals is continuous

$$\varphi_{S1}(r,L_1)=\varphi_{S2}(r,L_2) \tag{24-a}$$

$$\varphi_{S2}(r,L_2)=\varphi_{S3}(r,L_3) \tag{24-b}$$

At the edge of two different metals, the electric flux is,

$$\left.\frac{d\varphi_{S1}(r,z)}{dz}\right|_{at\ z=L_1}=\left.\frac{d\varphi_{S2}(r,z)}{dz}\right|_{at\ z=L_2} \tag{25-a}$$

$$\left.\frac{d\varphi_{S2}(r,z)}{dz}\right|_{at\ z=L_2}=\left.\frac{d\varphi_{S3}(r,z)}{dz}\right|_{at\ z=L_3} \tag{25-b}$$

Using the above boundary conditions, the values of the arbitrary constants in equation 19–21 can be obtained and written as

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$$O = \frac{V_{bi}(S)e^{\sqrt{\alpha}(L_1+L_2+L_3)} - V_{bi}(D) - V_{DS} + \frac{\beta_1}{\alpha}e^{\sqrt{\alpha}(L_1+L_2+L_3)} - \frac{\beta_2}{\alpha} + \left(\frac{\beta_2-\beta_1}{2\alpha}\right)Sinh(\sqrt{\alpha}(L_2+L_3))}{2Sinh(\sqrt{\alpha}(L_1+L_2+L_3))} \tag{26}$$

$$N = V_{bi}(S) - O + \frac{\beta_1}{\alpha} \tag{27}$$

$$U = Ne^{\sqrt{\alpha}L_1} + \left(\frac{\beta_2 - \beta_1}{2\alpha}\right) \tag{28}$$

$$V = \left(\frac{\beta_2 - \beta_1}{2\alpha}\right) + Oe^{-\sqrt{\alpha}L_1} \tag{29}$$

$$J = e^{-\sqrt{\alpha}L_3}\left[V_{bi}(D) + V_{DS} - Ke^{-\sqrt{\alpha}L_3} + \frac{\beta_3}{\alpha}\right] \tag{30}$$

$$K = \frac{(V_{bi}(D) + V_{DS})e^{-\sqrt{\alpha}(L_3+L_1)} + \frac{\beta_3}{\alpha}e^{-\sqrt{\alpha}(L_3+L_1)} - Ne^{\sqrt{\alpha}L_2} - \left(\frac{\beta_2-\beta_1}{\alpha}\right)Sinh(\sqrt{\alpha}\,(L_2 - L_1)) + Oe^{-\sqrt{\alpha}L_2}}{\sigma} \tag{31}$$

where. σ *is assumed to be* $= e^{-(\sqrt{\alpha}\,(2L_3+L_1))} + e^{\sqrt{\alpha}L_1}$

3.2. Electric filed model

From equation (19) – (21), by differentiating, the vertical direction electric field is given by

$$E_1(r) = \frac{-d\varphi_{S1}(r)}{dr} = \left(Ne^{r\lambda\sqrt{2}} - Oe^{r\lambda\sqrt{2}}\right)\lambda\sqrt{2}, \quad 0 \le z \le L_1 \tag{32}$$

$$E_2(r) = \frac{-d\varphi_{S2}(r)}{dr} = \left(Ue^{r\lambda\sqrt{2}} - Ve^{r\lambda\sqrt{2}}\right)\lambda\sqrt{2}, \quad L_1 \le z \le L_1 + L_2 \tag{33}$$

$$E_3(r) = \frac{-d\varphi_{S3}(r)}{dr} = \left(Je^{r\lambda\sqrt{2}} - Ke^{r\lambda\sqrt{2}}\right)\lambda\sqrt{2}, \quad L_1 + L_2 \le z \le L_3 \tag{34}$$

Similarly, the electric field for the lateral direction can be calculated by differentiating equations (3)–(5) with respect to 'z' which is given by $E_z = \frac{d\varphi_S(z)}{dz}$. Hence the total electric field can be obtained as

$$E = \sqrt{E_r{}^2 + E_Z{}^2}$$

3.3. Drain current model

The tunneling process of drain current is computed by using Kane's model [20], which describes the per unit volume generation rate. When the BTBT current contribution is significant, the TFET current can be calculated as the sum of overall charge produced in the device.

The drain tunnel current is given by

$$I_{ds-tun} = q\int_{TFET-Volume} G_{KANE}\, dV = q\int_{TFET-Volume} W\, L\, G_{KANE}\, dx \tag{35}$$

Where.

dV – elementary volume of the device, L,W- length and width of the gate, G_{KANE}-generation rate. The Kane's model obtained for a semiconductor with direct bandgap in a uniform electric field is given by,

$$G_{KANE} = A_{KANE}\frac{E^D}{\sqrt{E_g}}\, exp\left(-B_{KANE}E_g^{3/2} \Big/ E\right) \tag{36}$$

Where, A_{KANE}, B_{KANE} – material dependant constants, E-local electric field, E_g-bandgap, D-parameter separating the direct from the indirect tunneling process.

The average electric field over the tunnel path is given by,

$$E = \frac{E_g/q}{l_{path}} \tag{37}$$

Where, l_{path} – tunnel path length.

The following assumptions are made to determine the TFETs tunnel current by considering the electrostatic potential profile of TFET.

- The drain voltage has no effect on the potential profile in the region of the source channel where tunnelling occurs..
- The source doping for point tunnelling is high, so there is no depletion and potential drop in the source.
- There are no (inversion) charges in the channel and in the gate dielectric
- A gate dielectric with the same effective electrical thickness produces the same potential profile in the source and channel regions.

Tunneling of electrons is restricted in the proposed work by the assumption that tunnelling from the valance band to the conduction band is permitted only when starting from an energy level lower than the hole fermi level.

3.4. Potential profile

The electrostatic potential in the underlying semiconductor is strictly controlled by the gate. The effect of the drain voltage is found to be minor and can be ignored in the region directly beneath the gate. Adopting depletion region approximation.

The electric field obtained using depletion layer approximation is given by,

$$\varphi(z) = \frac{qN_a}{2\varepsilon_S}(x - x_{max})^2$$

For electrostatic potential, the electric field is expressed in terms of acceptor donor concentration

$$E(x) = -\frac{d\varphi}{dx} = -\frac{qN_a}{\varepsilon_S}(x - x_{max})$$

The tunnel current is determined by the potential profile in the source potential, which is perpendicular to the gate dielectric in line tunnelling.

As described, depletion layer approximation for potential profile is given by,

$$\varphi = 0 \quad ;for\ x < x_{max}$$

$$\varphi = \frac{qN_A}{2\varepsilon_S}(x - x_{max})^2\ ;\ for\ x > x_{max} \tag{38}$$

Where, N_A-source doping level, x_{max}-depletion starting position at source, ε_S- dielectric constant of the source.

To calculate $l_{path,}$ the x coordinate of points of equivalent potential in the valance band and conduction band are considered.

The value of $\varphi_V(x_1) = \frac{qN_A}{2\varepsilon_S}(x_1 - x_{max})^2 + \frac{E_g}{q}$; and

$$\varphi_C(x_2) = \frac{qN_A}{2\varepsilon_S}(x_2 - x_{max})^2$$

From the above equations tunneling path can be determined. The tunneling path length is given by.

$l_{path} = x_1 - x_2$, on equating $\varphi_V(x_1) = \varphi_C(x_2)$, it is obtained as

$$\left[\left((x_2 + l_{path}) - x_{max}\right)^2 - (x_2 - x_{max})^2\right] = \frac{2\varepsilon_S E_g}{q^2 N_A}$$

After simplification

$$x_2 \text{ can be computed as, } x_2 = x_{maxx} - \left[\frac{l_{path}{}^2 + 2E_g\varepsilon_S/q^2N_A}{2l_{path}}\right] \tag{39}$$

Differentiate the above equation with respect to tunneling path length, l_{path}

$$dx = -\frac{1}{2}\left(1 - \frac{2E_g\varepsilon_S}{q^2N_A} \times \frac{1}{l_{path}{}^2}\right)dl_{path} \tag{40}$$

Substitute the values of dx, E, G_{KANE} in equation (35) I_{ds-tun} can be obtained as

$$I_{ds-tun} = q\ W\ L\int_{l_1}^{l_2} A_{KANE}\frac{E_g{}^{D-1/2}}{q^D l_{path}{}^D}\ exp\left(-B_{KANE}\ q\ \sqrt{E_g}\ l_{path}\right)\ -\frac{1}{2}\left(1 - \frac{2E_g\varepsilon_S}{q^2N_A} \times \frac{1}{l_{path}{}^2}\right)dl_{path} \tag{41}$$

Where, l_1 and l_2 denote the maximum and minimum tunnel path length in the depletion region.

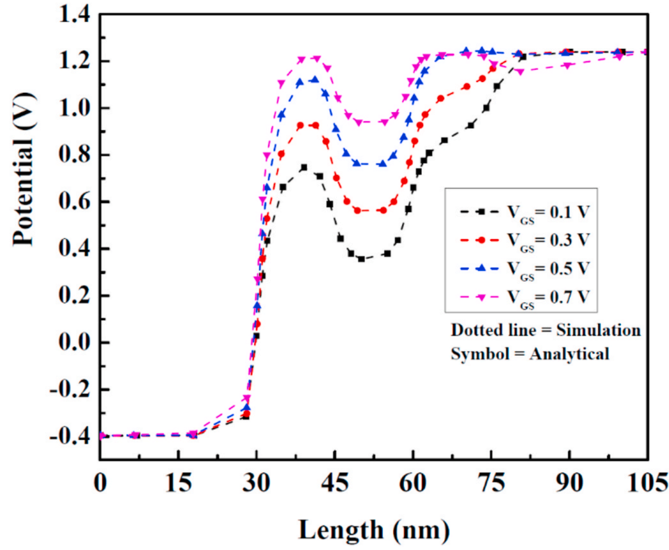

Fig. 5. Surface potential of SGTM-heTFET.

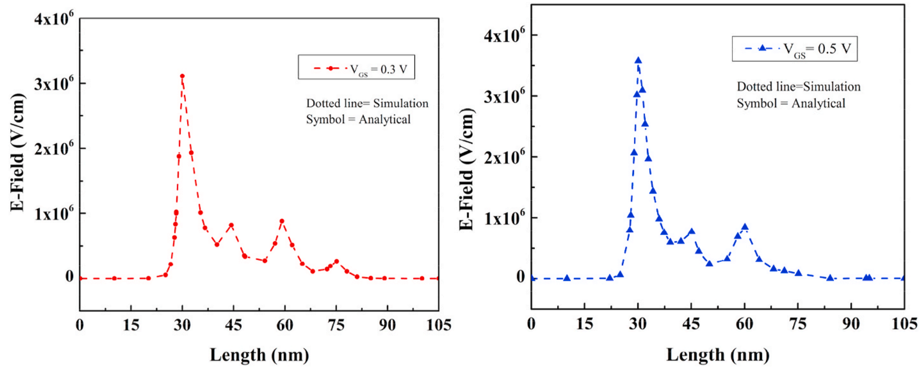

Fig. 6. Electric field of SGTM-heTFET with V_{gs} = 0.3V and 0.5V.

$$l_1 = \sqrt{\frac{2E_g\varepsilon_S}{q^2N_A}}\,;\; l_2 = \sqrt{\frac{2\varepsilon_S}{qN_A}}\left(-\sqrt{\psi_{max} - \frac{E_g}{q}} + \sqrt{\psi_{max}}\right)$$

Where, ψ_{max} – potential at the end of depletion layer.

The above integration can be simplified to an analytical formula by assuming that the exponent varies faster than the polynomial factors as tunnelling length varies(l_{path}.)

4. Results and discussions

In this section, we have displayed a few analytical model results with the corresponding TCAD simulation results to show the accurateness of the proposed model. In the simulation, band gap narrowing (BGN), Shockley–Read–Hall recombination (SRH), electric-field-dependent Lombardi, a non-local band to band tunnelling models have been adopted. Here high-k dielectric (HfO_2) oxide is used to decrease the leakage current through gate oxide layer and also to minimize the scattering due to phonons. The reason for SiO2 layer is to increase the carrier mobility. The surface potential, vertical electric field, lateral electric field and drain current calculated using analytical expressions are perfectly matching with the results simulated using TCAD simulation tool. The proposed triple material heterojunction surrounding gate TFET provides better electrical characteristics.

Fig. 5 provides the both analytical and simulated results of the surface potential for various gate to source voltages namely 0.1V, 0.3V, 0.5V and 0.7V. Increase in gate voltage results in increased potential in the lightly doped area. In the proposed stacked triple material surrounding gate TFET, there is an abrupt change in the potential through the channel in the interface region of source and the intrinsic region. The figure clearly shows that owing to the close proximity of gate bias, there is a revolutionary change in the potential below the gate and which gives a major improvement in surface potential which leads to improved tunneling current. Simulated results

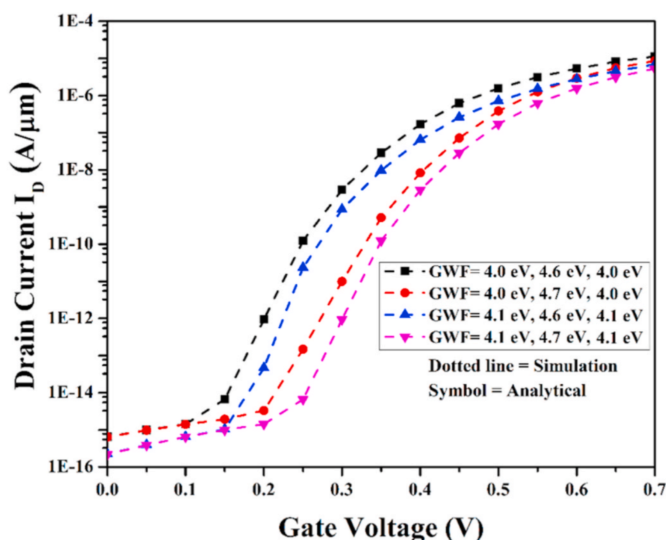

Fig. 7. I_D - V_{GS} plot of Surrounding Gate Triple Material heterojunction TFET for different Gate work functions.

give better accuracy with the analytical results.

The different electric field profiles along the channel with various gate to source voltages (V_{GS} = 0.3V & 0.5V) are shown in Fig. 6. Apart from the source-channel junction, the electric field is very minimum for the entire channel area and it is getting some peak values at the junction of different gate materials. It is observed that the peak value of the electric field occurs at the interface region of source and channel with the value of $3x10^6$ V/cm, which is the reason for the tunneling from source to channel and higher gate voltage achieves better electric field at the tunnelling junction with increasing the tunnelling probability. The reason for the peak at the drain side is due the drain influence of drain potential. The same results have also been related with the simulated one to check the correctness of the analytical one.

The drain current against gate voltage for different metal work functions are shown in Fig. 7. The results obtained by the model is in good match with the simulated one. The figure compares four different plots by keeping $\varphi_{M1} = \varphi_{M3}$ = 4.0eV and by varying the φ_{M2} as 4.6eV and 4.7eV. Similarly, by keeping $\varphi_{M1} = \varphi_{M3}$ = 4.1eV and by varying the φ_{M2} as 4.6eV and 4.7eV. Due to the use of various gate material work functions, the vertical electric field is increased. Further, the use of material with a low work function on the source side results in a shortening of the tunnelling width, which improves the ON current. As stated above, the plot of V_{GS} versus I_{ds} with the work functions of 4.0eV, 4.6eV and 4.0eV gives better ON current of 10^{-5} A/μm, and the ON-OFF ratio of 10^{10} and also the sub-threshold swing is measured as 50mV/dec when compared with the other three combinations.

5. Conclusion

In this work, an analytical model of surface potential, electric field and drain current have been developed for the proposed triple material surrounding gate TFET with HfO_2/SiO_2 stacked arrangement. The use of stack arrangement is to expand the control of gate along the channel, and thereby to increase the tunneling current. The drain current is calculated numerically using both the lateral and vertical electric fields. The analytical model results have been compared with the simulated results which show a better accuracy. This new device structure doubtlessly predicts enhanced gate control and shows remarkable characteristics and also with the help of work function engineering, it has a higher drain current than its TFET counterparts.

Author statement

M.Sathishkumar: Conceptualization, Methodology and Writing – original draft preparation. T.S.Arun Samuel: Supervision, K. Ramkumar: Simulation. I.Vivek Anand: Writing – review & editing: S.B.Rahi: Checked the comparison results and Validation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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