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A review on emerging negative capacitance field effect transistor for low power electronics

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ABSTRACT

Power consumption is the major concern for conventional CMOS based integrated circuit and systems. Since there is a scope of lowering supply voltage with steep-subthreshold swing field effect transistor (FET) devices, it has been advocated as a suitable candidate for future highly energy-efficient circuits and systems. Among all the developed and proposed low power FET devices, that possess subthreshold swing (SS) lesser than 60 mV/decade, the negative-capacitance FETs (NCFETs) have gained the major attention of scientific and academic communities. The concept of negative capacitance (NC) in FET is basically belongs to the amplify the internal potential without modification of transport phenomena. With this capability, the NCFET have achieved similar switching at lower supply voltage, V_{DD} as compared to conventional MOSFETs. Property of achieving similar on-current (I_{ON}) lower off-current (I_{OFF}) at lower supply voltage indicates that NCFETs help to reduce the power consumption and switching voltage. This can be achieved by slight modification of conventional CMOS devices by adding thin layer of ferroelectric (FE) layer in gate stack. This slight modification in conventional MOSFET is for the NC, which is a special feature of FE materials. FE materials having nonlinear dielectric behavior. This material has preexisting, which is switched in reverse direction when an external electric field is applied. In this paper, a detailed review of NCFET device has discussed and also compared with the Tunnel FET (TFET) and conventional MOSFET.

1. Introduction

The thermal and power management of integrated circuits (ICs) are the most important concern for the semiconductor industry. Although with the advancement of material science and engineering technology an individual transistor produces a very small amount of heat. However the ICs have billion of transistors in a single chip, which collectively produces huge amount of heat and becoming the bottleneck concerns for scientists and engineers [1–15]. The supply voltage reduction is one of the most effective technique to solve this issue. Because there is the square of supply voltage dependency of power factor ($i.e. P_{dyn} \propto V_{DD}^2$). For conventional MOSFET, the rigorous scaling of supply voltage (V_{DD}) technique reached to fundamental limits of 60 mV/$decade$, so-called "Boltzmann Tyranny" [10–20].

There will several ways through which the semiconductor devices are classified. But here we have put all together developed FET devices only with reference to subthreshold swing (SS). As shown in Fig. 1, field effect transistors community have been classified in two groups. One group having SS larger than 60 mV/$decade$ and other group having less than this value. In case of bulk MOSFET, FDSOI, FinFET, and NWFET conventional MOSFET device technology. The numeric value of this fundamental of conventional CMOS technology is ~ 60 mV/$decade$ [10–15] at room temperature. The minimum possible, V_{DD} is limited due to subthreshold swing SS of $V_{DD} \geq SS \times \log_{10}(I_{ON}/I_{OFF})$. In this conceptual V_{DD} scaling limitation, I_{ON} and I_{OFF} having usual meaning, denoted current in on and off-state. To break the barrier of "Boltzmann Tyranny", various alternative device architectures such as tunnel FETs, NCFETs, NCTFETs and impact-ionization MOSFETs have been presented [10–22].

Aforementioned devices motivates the researcher to continue work on the principle of "scaling" of MOFET devices. It is expected that this proposed device helps to resolve that power issue and thermal management of large-scale application in ICs. Because total power consumption, $P_{total} = P_{static} + P_{dynamic}$ and dynamic power consumption followed the relation, $P_{dynamic} = \alpha C_{total} V_{DD}^2 f$. The supply voltage scaling also helps to reduces the switching energy, followed by $\alpha V_{DD}^2(\epsilon + I_{OFF}/I_{ON})$, here ϵ is active time ratio. The standard ϵ value is chosen

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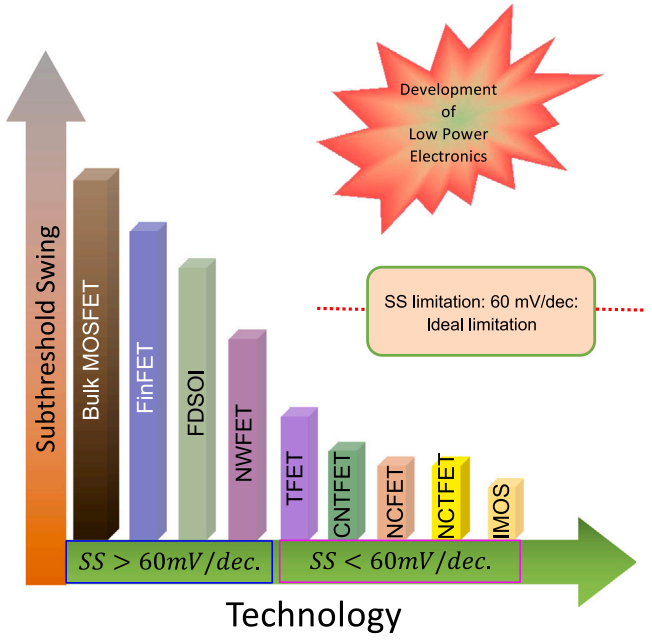

Fig. 1. Progress of semiconductor field Effect transistors.

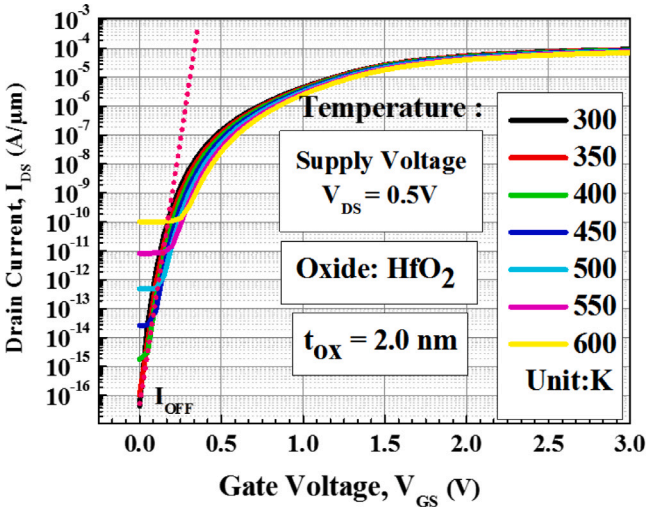

Fig. 2. Thermal impact on transfer characteristics of TFET.

1/800 for logic circuit and 1/10000 for memory [23]. As shown in Fig. 1, among all subthreshold swing devices developed by experts, Tunnel FET and NCFET devices have a strong attention because of their lower SS, and operating supply voltage [24–34].

Around one-decade, various research groups in device community have started to claims that tunnel FETs are most suitable substitute of conventional MOSFETs for future lower power applications, due to lowered I_{OFF} and lower supply voltage [15–22,35–37]. TFET is basically p-i-n based device has lower SS (*i.e.*, $SS < 60$ mV/$decade$) than conventional FETs like bulk MOSFET, FinFETs, FDSOI. Naima et al. [19] and A. M. Ionescu [18] reported that thermal study of double gate TFET. The thermal sensitivity results shown in Fig. 2 of TFETs shows it is suitability for various thermal hazardous applications, where conventional FETs is not working properly. However, the major concern of TFETs is its low I_{ON} which is limited due to band-to-band (B2B) tunneling, forces to think further improvement in this FET device [1,4,17–21,38–43]. Various research groups continuously working to resolve this limitation, but till now no one have gain success. Thanks to the identification and incorporation of negative capacitance in material technology by Prof. S. Salahuddin and Datta in 2008 [24,44–47].

The adoption and implementation of concept of NC in MOS devices have been incorporated for support of requirement of ultra low power ICs. Available literature reports that NCFET device have sufficient potential to overcome the existing limitations of conventional MOS technology. As well as, it have super features than other SS devices likes TFET and IMOS. Because, NCFET devices not suffering with low on-state current and working on lower supply voltage than (IMOS) [25–34,38–43,48–51]. To achieve the ferroelectricity and NC, a thin layer of FE material is added in gate stack. This added additional FE layer help to amplify the surface potential of MOSFET, reduces threshold voltage and maintain the I_{ON} current as compared to classical CMOS technology without compromising with, I_{OFF} [42,43,49–61]. This indicates that NCFET devices consume less power without any loss of switching speed.

In this review paper, we briefly summaries the bottleneck issues of conventional CMOS technology and alternative option as NCFET. This review paper presented by keeping in mind the fundamental requirements of new researchers in the field of device, engineering and technology. The collective information in this paper is expected to provides basic understanding of NCFET device physics and its impact. The reported results in this review paper are basically a qualitative analysis for representing the necessity, progress and future impact of NCFET technology for the development of low power device, circuit and system.

2. Limitation of conventional MOSFET and future scope: Mechanism toward steep subthreshold swing technology

Nowadays the SS is becoming the fundamental parameter for low power devices, used for determining the operation in sub-threshold regime. In the classical MOSFET, subthreshold slope is defined as, $S = (\log_{10}(I_{DS2}/I_{DS1}))/(\Delta V_{gs})$, while $\log_{10}(I_{DS2}/I_{DS1})$ is rate of change of drain current, corresponding, ΔV_{gs}. The SS of FET device is inverse of subthreshold slope. For classical MOS devices ~60 mV/$decade$ at 300 K, known as "Boltzmann Tyranny" [23,62–70]. To overcome this limitations researchers invented and developed various FET devices having steep subthreshold swing feature. The SS of classical MOS devices is modeled as:

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_{gs}}\right)^{-1} = \frac{dV_{gs}}{d\psi_s} \times \frac{d\psi_s}{d(\log_{10} I_{DS})} = \left(1 + \frac{C_d}{C_{ox}} \times \frac{d\psi_s}{d(\log_{10} I_{DS})}\right) = m \times n \quad (1)$$

In Eq. (1), SS is product of body factor and transport factor, denoted as "m" and "n" respectively. The term "m" defined as $(1+C_d/C_{ox}) \gg 1$, due to "positive" series connected gate oxide capacitance (C_{ox}). This shows that, the body factor for classical MOS devices is always greater than one. In Eq. (1), the term "n" is basically using for determining the band bending due to applied gate voltage. The development of NC concept in MOS device does not change the carrier transport phenomena of charge carriers. It only amplifies, the internal surface potential (ψ_S) in term of gate voltage by involvement of thin layer of ferroelectric materials in structure such as conventional MOSFET and TFET structures, known as NCFET and NC TFET respectively [71–84].

In expression "SS" the factor "n" of Eq. (1) for conventional MOSFET is mathematically modeled by Eq. (2),

$$n = \frac{d\psi_S}{d(\log_{10} I_{DS})} = \log(10) \times \frac{k_B T}{q} = 2.3 \times 25.8 \ \frac{\text{mV}}{decade} \approx 60 \ \frac{\text{mV}}{decade} \quad (2)$$

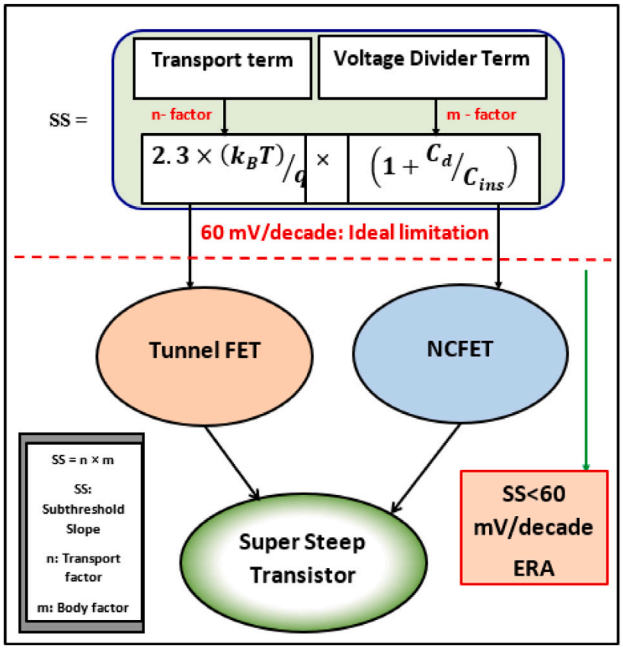

Fig. 3. Future scope of steep subthreshold slope devices.

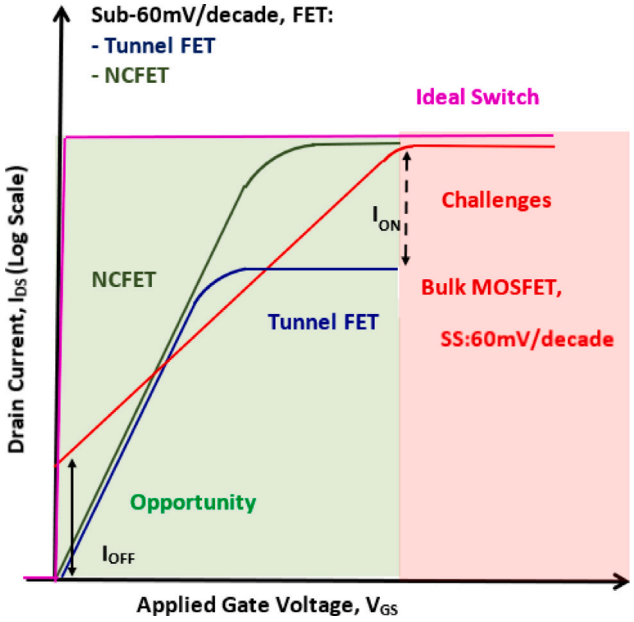

Fig. 4. Comparison of transfer characteristics of popular device, TFET and NCFET with conventional MOSFET.

This ideal limitation in conventional FET structure such as bulk MOSFET, SOIFETs, FinFET, created a great bottleneck problem for CMOS technology. The modern semiconductor players have proposed and developed various FET device for next-generation applications to get rid of ~ 60 mV/$decade$ issue. However in real scenario, among all devices, only two field effect transistors namely NCTFET, and NCFET gains more attention. NCTFET is upgraded version of conventional TFET. Fig. 3 graphical representation of the development flow of modern low power electronics and future scope.

The qualitative investigation of most popular steep SS device such as NCFET, TFET, and bulk MOSFET are shown in Fig. 4. As shown in Fig. 4, the newly developed novel devices like NCFET, and Tunnel FET having lower SS, desirable I_{ON} and low I_{OFF}.

On the basic of reported scientific evidences, a qualitative analysis shown in Fig. 4, NCFET is treated as a super switch for modern electronics due lower subthreshold swing, higher I_{ON} than its relative competitor TFET and comparable to classical MOSFET at lower supply voltage. As shown in Fig. 4, the Tunnel FET suffers from low drive current, I_{ON} which limits its applications design performance such as lower g_m and I_{ON}/I_{OFF} ratio and g_m/I_{DS} power factor for technology. Due to lower g_m values its linearity performance is also limited for high frequency applications. Practically, in case of NCFET and Tunnel FET, off-state switching current is much lower than conventional MOSFET [43,56,67–69].

In NCFET, ferroelectricity property of ferroelectric material has been incorporated in gate region [44,45,49]. NC is basically, change the charges due to applied voltage in opposite direction. It causes a decrease in voltage leads to an increase in charge known as internal voltage amplification (β), is

$$\beta = \frac{\partial V_{int}}{\partial V_{gs}} = \frac{C_{EF}}{C_{EF} + C_{int}} \gg 1 \tag{3}$$

where, ∂V_{int} is the.

The relation between body factor "m" and internal gain β for NCFET is defined by Eq. (4).

$$m = \frac{1}{\beta} \times \frac{\partial V_{int}}{\partial \psi_S} = \frac{1}{\beta} \times \left(1 + \frac{C_S}{C_{ox}}\right) \ll 1 \tag{4}$$

With conventional CMOS technology in short channel devices, subthreshold swing and DIBL increases rapidly with scale device gate length. While in case of NCFET, the behaviors are just opposite to conventional devices such as negative DIBL, having low SS and output resistance also become negative as L_g scaled down [23,51–70]. For achieving more gate control, lowering SS and power factor of complex circuit and system, the present semiconductor industry is dedicated to NC [23,70,81].

On the basic of "m" and "n" factor semiconductor device are classified into four domains:

- **Category No 1:** In domain 1, if $n > 60$ mV/$decade$ and $m > 1$. Classical MOS Devices like bulk MOSFET, FinFET lies in this domain.
- **Category No 2:** In this domain, for $n < 60$ mV/$decade$ and $m > 1$. Tunnel FET and IMOS lies in this category.
- **Category No 3:** In third domain, $n > 60$ mV/$decade$ and $m < 1$. Negative capacitance FET device lies in this domain. Electromechanical devices are common example of this category.
- **Category No 4:** Fourth domain, where $n < 60$ mV/$decade$ and $m < 1$.

The transfer characteristics of TFET shown in Fig. 4. It has been observed that low off current helps in suppressing the dynamic power dissipation while low on-state current is not good for fast switching. This affect I_{ON}/I_{OFF} also lower g_m than conventional value which is an essential design parameter for digital circuits and system. Fig. 4 shows that NCFET overshoot the limits of Tunnel FET and conventional MOSFET. The lower g_m value than classical MOSFET and NCFET indicates that tunnel FET having lower cut-off frequency, f_T and gain bandwidth, GBW estimated by $f_T = g_m/2\pi(C_{gs} + C_{gd}) = g_m/(2\pi C_{gg})$ and $GBW = g_m/(2\pi 10 C_{gd})$ respectively. The both design parameters are directly proportional to g_m. Also, for analog and RF applications, linearity measured by its higher order derivative i.e., $g_{mn} = \frac{1}{n!}\left(\frac{\partial^n I_{DS}}{\partial V_{gs}^n}\right)$, where n=1,2,3... are order also reduces.

NCTFET is basically advanced version of conventional tunnel FET having additional thin layer of FE materials in gate stack. In NCTFET, transport of charge carriers in controlled by popular WKB quantum theory, given in Eq. (5). Fig. 5, shows the B2B tunneling of TFET. In TFET the tunneling current is directly proportional to the tunneling probability ($T(E)$). Now the combination of B2B tunneling and NC

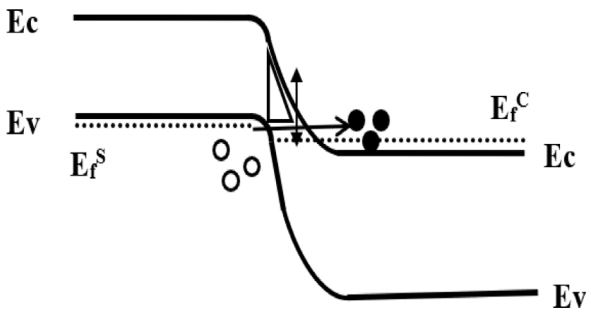

Fig. 5. Simplified picture of B2B tunneling in TFET.

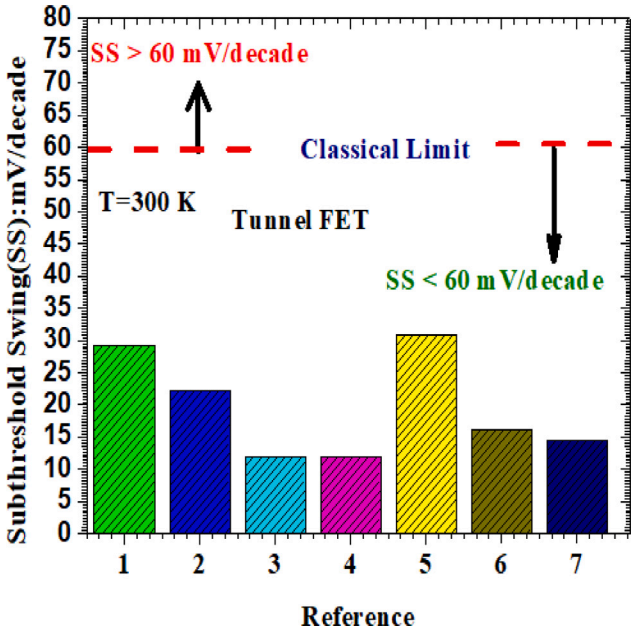

Fig. 6. Subthreshold Swing of reported TFET.

feature of ferroelectric materials, helps to reduce the transport factor "n" as well as body factor "m" [23,59–72]. This combined mechanism of NCTFET plays a crucial role for further development of ultra-low power device [17,20,51]. The $T(E)$ is used for estimation of quantum band to band tunneling.

$$T(E) \propto \left(-\frac{4\sqrt{2m^*}E_{g-effective}^{\frac{3}{2}}}{3|q|\hbar(E_{g-effective}+\Delta\Phi)}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}} \right)\Delta\Phi \tag{5}$$

where, m^* is effective mass, $E_{g-effective}$ is effective band gap, $\Delta\Phi$ is tunneling window, ϵ_{Si}, ϵ_{ox} is dielectric constants of Si and oxide material respectively, and t_{si}, t_{ox} is thickness of Si and oxide material respectively.

The tunneling window can be expressed as: $\Delta\Phi = E_{VB}^{ch} - E_{CB}^{S}$. As shown in Table 1, the reported temperature sensitivity for double gate tunnel FET having SiGe and Si source, channel material has been presented. Table 1 indicate that impact of I_{ON} is negligible, however slight variation in I_{OFF} has been obtained. It is expected, this is due to intrinsic and gate leakage cause this slight variation is I_{OFF}. However, due to low on-state current, TFET is not expected as suitable in high speed, low power application. Fig. 6 shows the reported subthreshold swing for TFET [1–7]. Reported information in Fig. 6 and Table 2 provides the comparison of its lower SS than 60 mV/$decade$, I_{OFF} while existence of also low I_{ON}.

Moreover, the most challenging task for TFETs is their reliability. Mismatch arising from the process fabrication will degrade the device

Table 1
Temperature variation effect on TFET.

Temp. (K)	I_{ON} (A/μm)	I_{OFF} (A/μm)
300	9.29×10^{-6}	4.32×10^{-17}
350	8.96×10^{-5}	1.04×10^{-16}
400	8.57×10^{-5}	1.78×10^{-15}
450	8.21×10^{-5}	2.63×10^{-14}
500	7.85×10^{-5}	4.89×10^{-13}
550	7.51×10^{-5}	8.43×10^{-12}
600	7.19×10^{-5}	1.05×10^{-10}

Table 2
Reported information of TFET.

$V_{DD}(V)$	I_{ON} (A/μm)	I_{OFF} (A/μm)	Reference
0.5	~1.0	1.0×10^{-10}	[38]
0.5	~10.0	1.0×10^{-10}	[38]
0.5	~9.96	1×10^{-8}	[39]
0.3	~177	1.0×10^{-11}	[41]
0.3	~366	1.0×10^{-12}	[41]
0.3	~328	1.0×10^{-14}	[41]

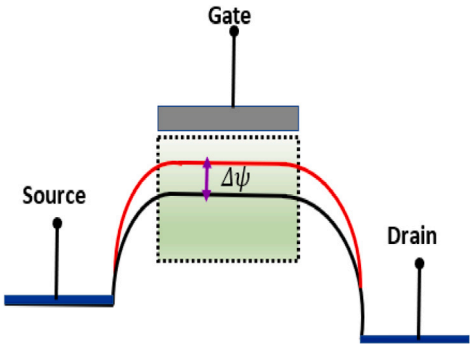

Fig. 7. Impact of negative capacitance in surface potential.

and circuit performance at some extent. So, investigating the mismatch property of NCFET is also necessary, which have been investigated by Liang et al. [85]. They analyzed the process variation of the dimensions and polarization of ferroelectric film on the performance of NC-FET based 5-stage ring oscillator and current mirror. They concluded that the degrade in device/circuit performance of NC-FET devices is not much severe.

3. Negative Capacitance FET (NCFET): Principle & operation

3.1. Basic principle of NC FET technology

The working principle of NCFET is based on passive internal gate voltage amplification due to ferroelectric depolarization. The surface potential ψ_S in NCFET relatively larger than conventional MOSFET under same operating condition. This device technology does not change any charge transport phenomena like TFET, only add internal voltage amplification, as shown in Fig. 7 [14–17,35,44]. It is such type of device which utilizes non linearity of its gate insulator. NC effect arises from negative coefficient around the metastable state can be stabilized by connecting paraelectric capacitor in series ferroelectric [86], [87].

3.2. Origin of NCFET

The concept of NC is jointly proposed by S. Salahuddin and Datta for conventional CMOS technology. In order to implement this novel idea, they have deposited a thin layer of FE material is used in place of dielectric layer in gate stack of conventional MOS, to overcome the limitation of conventional CMOS technology [24–28,44–47]. The

modification in conventional MOSFET architecture allow to operate at a lower supply voltage [24–32,46,47].

The SS of a classical MOSFET is expressed by following Eq. (6).

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_{gs}}\right)^{-1} = \frac{d\psi_{GS}}{d\log_{10} I_{DS}} \times \frac{dV_{gs}}{d\psi_{GS}} = 60 \times \left(1 + \frac{C_S}{C_{ox}}\right) \quad (6)$$

From Eq. (6), it has been observed that, this relation contains two material capacitances, one is associated with the gate oxide capacitance (C_{ox}), while another is substrate capacitance (C_S) [24–29,37,44–47].

In order to achieve lower SS than 60 mV/$decade$, ($1+C_S/C_{ox}$) should be less than 1. Practically it will be possible only if

$$C_{ox} < 0; \quad |C_{ox}| > C_S \quad (7)$$

The condition shown in Eq. (7) mean that C_{ox} must be negative and C_S must be appropriately designed to be less than $|C_{ox}|$. In conventional MOSFET, practically, it is not possible. But in case of NC FET technology, it is feasible due to negative capacitance in ferroelectric materials. In ferroelectric materials, the polarization phenomena versus applied electric field shows like S-shaped, P–E curve. In the P–E curve, clearly, there exist negative slope between applied field. This ferroelectric material property overall reduces the body factor $m < 1$ as well as SS. This unique material property has found much more attraction in semiconductor industry.

4. Modeling of ferroelectric materials for NC FET applications

4.1. Landau–Khalatikov (L–K) equation

L–K and Miller models are commonly used methods for explaining the polarization $\vec{P}$ and voltage across FE materials [29–32]. But L–K has gained more attention. In this section, we have discussed about L–K model. Landau–Khalatnikov (L–K) equation is a dynamical version of Landau–Devonshire theory. The L–K equation is most effective tool to understand the ferroelectric switching properties in NC FET technology development [29–32,44].

The explanations of negative capacitance (NC) are based on the L–K equation, where the steady-state relation between polarization ($\vec{P}$) and voltage (V) has a negative derivative $\vec{P}/dV$ region. The time evolution of the polarization $\vec{P} = (P_x, P_y, P_z)$ in a ferroelectric material is described in L–K model. The L–K model for the charge–voltage characteristic of the ferroelectric material is characterized as:

$$\lambda \frac{\partial \vec{P_i}}{\partial t} = -\frac{\partial G}{\partial \vec{P}} \quad (8)$$

here, λ is a kinetic coefficient, ($\vec{P}$) is the polarization charge per unit. The thermodynamic energy (G) can be written in the Landau–Devonshire model as

$$G = \int_V g dV \quad (9)$$

where,

$$g = \alpha(P_x^2 + P_y^2 + P_z^2) + \beta(P_x^4 + P_y^4 + P_z^4) + \gamma(P_x^6 + P_y^6 + P_z^6) - \vec{P} \cdot \vec{E} \quad (10)$$

The relationship of polarization $\vec{P}$ to the electric field $\vec{E}$ in steady state is given by

$$2\alpha P_i + 4\beta P_i^3 + 6\gamma P_i^5 - \vec{E_i} = 0 \quad (11)$$

In conventional dielectric materials, the Poisson's equation is known as governing relation, used for measuring polarized charge and electric field, written as

$$\nabla \cdot \vec{D} = 0 \quad (12)$$

In a paraelectric, $\vec{P}$ is proportional to E and can be encapsulated in permittivity ϵ

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P} \approx \epsilon_0 \vec{E} + \chi \epsilon_0 \vec{E} = \epsilon \vec{E} \quad (13)$$

and

$$\nabla \cdot (\epsilon \vec{E}) = 0 \quad (14)$$

While, in case of ferroelectric, $\vec{P}$ is not proportional to $\vec{E}$. In case of Ferroelectric's behavior is governed by Eq. (15)

$$\nabla \cdot (\epsilon \vec{E} + \vec{P}) = 0 \quad (15)$$

Now modified Poisson's equation

$$2\alpha P_i + 4\beta P_i^3 + 6\gamma P_i^5 - E_i = 0 \quad (16)$$

The dynamic behavior of ferroelectric, material has been model by L–K model. Basically, the L–K equation is the rate of change in polarization charge $Q_{FE} = \vec{P}A$ in the ferroelectric (FE), where $\vec{P}$ is the polarization and A is the cross-sectional area,

$$\rho \frac{dQ_{FE}}{dt} = \frac{dU}{dQ_{FE}} \quad (17)$$

In Eq. (17), ρ is the switching resistivity that determines the dynamic response of the polarization in the FE material, G is the Landau free energy, and α, β, and γ are the Landau parameters that determine the static property of the FE material. Here, $\rho > 0$ signifies the frictional inertia of the system and U (in electron volts) is the free energy of the FE material that can be written as:

$$U = \frac{\alpha}{2} Q_{FE}^2 + \frac{\beta}{4} Q_{FE}^4 - Q_{FE} V_{FE} \quad (18)$$

where α and β are anisotropy ($\alpha < 0$) and V_{FE} is the voltage across the FE capacitor. For simplicity, we have only included up to the fourth order of Q_{FE}, which corresponds to a second-order phase transition. By combining Eqs. (17) and (18), we have following. Eq. (19).

$$V_{FE} = \rho \frac{dQ_{FE}}{dt} + (\alpha Q_{FE} + \beta Q_{FE}^3) \quad (19)$$

in the steady state,

$$V_{FE} = \alpha Q_{FE} + \beta Q_{FE}^3 + \gamma Q_{FE}^5 \quad (20)$$

Eq. (14) can be written in term of t_{FE}

$$V_{FE} = t_{FE}(2uQ_{FE} + 4vQ_{FE}^3 + 6\omega Q_{FE}^5) \quad (21)$$

where, t_{FE} is thickness of ferroelectric material and α, β and γ are material dependent parameters. The NC effect occurs, when polarization switching current ($d\vec{P}/dt$) exceeds free carrier displacement current (dQ/dt). When ($d\vec{P}/dt$) largely increases, dQ/dt through a small depletion layer capacitance in subthreshold region cannot fully balance. Then the voltage across ferroelectric gate insulator is reduced, which results in depolarization effect.

Now, if we assume that the higher order terms of Eq. (21) are negligible, then we can write.

$$V_{FE} = 2uQ_{FE}t_{FE} \quad (22)$$

In general, the gate to source voltage, V_{gs} in NC FET is due to ferroelectric materials.

$$V_{gs} = V_{MOS} + V_{FE} \quad (23)$$

The relation, $V_{gs} = V_{MOS} + V_{FE}$, expressed in Eq. (22) indicates that external applied voltage is material dependent used as FE materials. By using Eq. (21) and Eq. (23), the gate to voltage relation becomes

$$V_{gs} = V_{MOS} + t_{FE}(2uQ_{FE} + 2vQ_{FE}^3 + 6\omega Q_{FE}^5) \quad (24)$$

From Eq. (24), it is evident that in NCFET technology, gate to source voltage is material parameter dependent of Landau coefficient (α, β, γ) and thickness of ferroelectric materials. Table 3 summaries some popular ferroelectric materials.

Fig. 8, shows the polarization phenomena under applied electric field for FE materials. Mathematical analysis shows that P–E curve can obtain using desired FE materials, having specific L–K variables α, β and

Table 3
Landau coefficient (α, β, γ) for ferroelectric materials [1–14].

Material	α-value [m/F]	β-value [m^5/F/$Coul^2$]	γ-value [m^9/F/$Coul^4$]
$BaTiO_3$ (BTO)	-1.0×10^7	-8.9×10^9	4.5×10^{11}
HfZro	-7.0×10^8	1.0×10^{12}	0.0
SBT	-1.3×10^8	1.3×10^{10}	0.0
HfSiO(1)	-4.0×10^8	-5.1×10^{10}	3.7×10^{12}
HfSiO(2)	-1.45×10^9	-2.5×10^{12}	2.45×10^{15}
P(VDF-TrFE)	-1.98×10^9	-3.75×10^{11}	3.16×10^{13}
PZT (1)	-4.24×10^8	2.3×10^8	3.8×10^{10}
HZO	-7.0×10^8	1.0×10^{12}	0.0
Y-HfO_2	-1.23×10^9	3.28×10^{10}	0.0
PZT (2)	-1.48×10^8	-3.0×10^7	2.47×10^8
$Pb(Nb_{0.04}Zr_{0.28}Ti_{0.68})O_3$	-5.37×10^7	-3.0×10^7	2.47×10^8

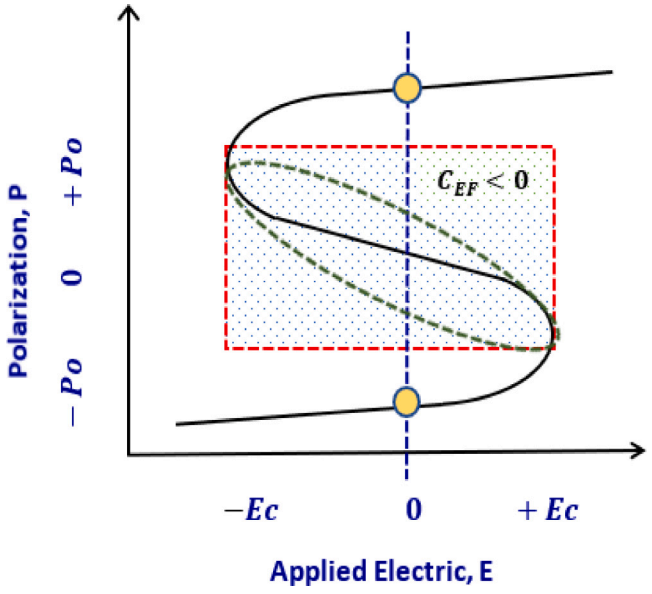

Fig. 8. Polarization versus electric field.

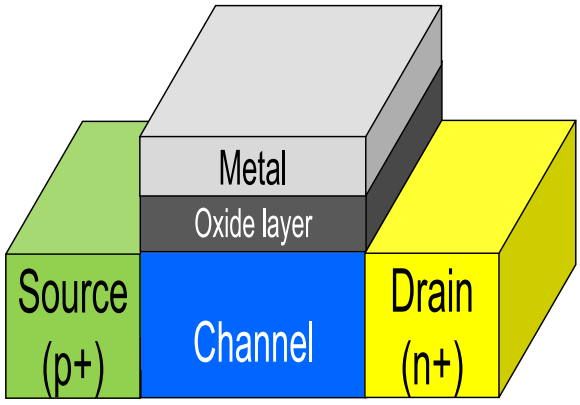

Fig. 9. Simplified schematic diagram of n-TFET.

γ. From Fig. 8, it has been noticed that, $(d\overrightarrow{P})/dE < 0$, play a vital role in NCFET as voltage amplification. When the gate voltage increases, the ferroelectric voltage drop decreases because $(d\overrightarrow{P})/dE < 0$, then surface potential is naturally amplified.

As shown in Fig. 8, the shaded rectangle denotes the cross-sectional area (A) of FE material. The change in polarized charges due to applied electric field (E) that is $(dQ_{FE})/dE \approx (dQ_{FE})/dE$ between $-E_C$ to $+E_C$ having negative slope. In other word, we can say that, this is basically rate of change store charges with applied voltage i.e. $(dQ_{FE})/(dV_{FE})$. Negative slope with applied voltage in FE material is evidence of "Negative Capacitance".

5. Impact of ferroelectric material and negative capacitance in field effect

5.1. Impact of negative capacitance: state-of-the art

Among all SS devices, TFETs and NCFETs have gained more attention than other devices like IMOS [15–17]. This is because, these devices have operated at lower supply voltage with optimum drive current and low I_{OFF}. While major roadblock of TFETs are suffering with low on-state current and higher ambipolar current (I_{amb}) [18,67], this is due to quantum transport, band to band tunneling. In Tunnel FET there are little bit compatibility issue also with conventional MOSFET. Because, as it is known that conventional CMOS devices, there are uniform and same source and drain doping. The source and drain terminal can be interchange in case of conventional CMOS and its relative development like FinFET and SOI. While in case of TFET structures, n-TFET having highly doped p-region known as source and highly doped n-region known as drain. This indicates like conventional MOSFET, source and drain terminal cannot interchange, as per our simplicity during complex circuit and system design. The simplified pictorial schematic diagram of conventional n-TFET is shown in Fig. 9.

Meanwhile the development of negative capacitance in FE materials showed an important tool to bypass the conventional MOS device limitation of 60 mV/$decade$. The integration of negative capacitance in tunnel devices look like supremacy. It would be highly beneficial for energy band bending due to the internal voltage amplification helpful for enhancing the B2B probability in TFETs and reduces threshold voltage of conventional MOS structure. A negative capacitor in the gate stack can make the total capacitance larger than its classical value followed by Eq. (25), which leads to the decrease of the required ΔV_{gs} to provide the same $\Delta\psi_S$.

$$C_{total} = \left(C_{FE}^{-1} + C_{int}^{-1}\right) \tag{25}$$

The internal amplification factor, β in NC FET technology is defined as:

$$\beta = \frac{\partial V_{int}}{\partial V_{gs}} = \frac{C_{FE}}{(C_{FE} + C_{int})} \gg 1 \tag{26}$$

Fig. 10(a) shows the schematic of conventional NCFET, Fig. 10(b) is its equivalent model. While the C–V model of this device is shown in Fig. 10(c). In equivalent NCFET model, additional capacitance C_{FE} due thin layer of ferroelectric material is added in series with conventional MOSFET.

Fig. 10(c). NC FET transistor voltage capacitance model V_{gs1} and V_{gs2} are voltage denoted at gate electrode and internal gate of NCFET. As per theory of NCFET, $V_{gs1} = \beta \times V_{gs2}$, where β is internal gate amplification. Initially, this amplification factor is depending on material property of ferroelectricity.

Fig. 11 shows qualitative analysis of transfer characteristics between NCFET versus Tunnel FET. From Fig. 11 it has been observed that,

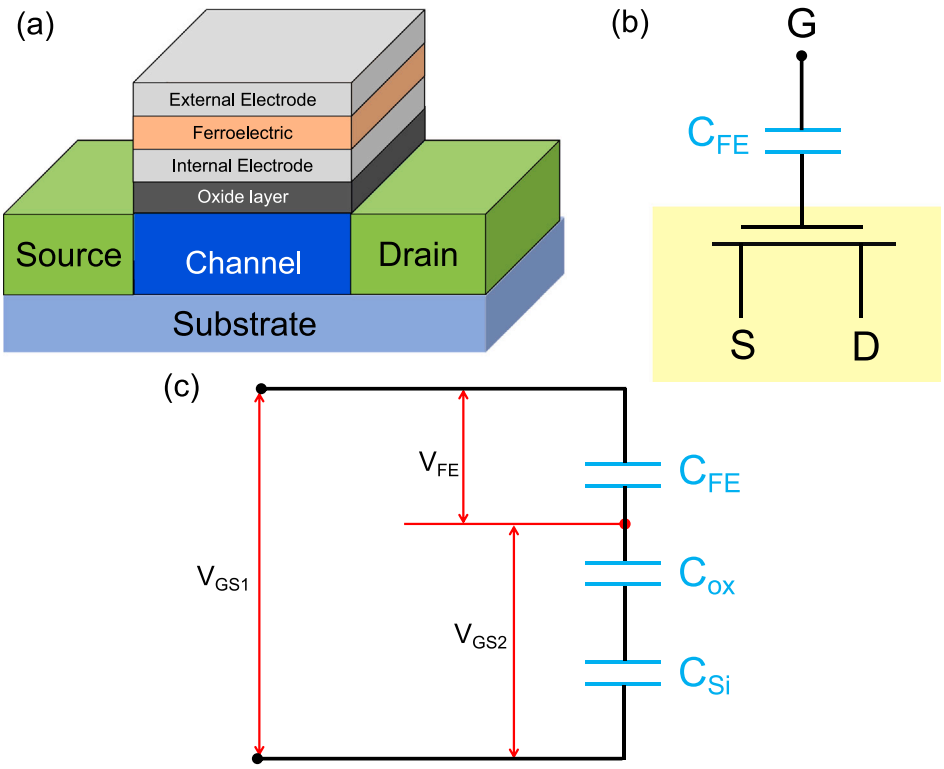

Fig. 10. (a) 3D view, (b) symbol, and (c): capacitance model of NCFET.

Table 4
Review report negative capacitance FET.

V_{DD} (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS mV/decade	Ref.
–	~100	–	13	[1]
0.3	~250	1.0×10^{-11}	21	[2]
0.2	~600	–	34	[3]
0.4	~100	$1.0 \times \sim 10^{-8}$	–	[4]

Table 5
Review report Tunnel Field Effect Transistor (NC TFET)

V_{DD} (V)	I_{ON} (μA/μm)	I_{OFF} (A/μm)	SS mV/decade	Ref.
0.5	~40.5	1×10^{-11}	13.8	[1]
1.0	~10	–	20	[3]

I_{OFF} is almost same in both field effect transistor, while switching I_{ON} current with Tunnel FET is lowered as compared to NCFET, due to B2B tunneling.

One important consequence of NCFET is it's a large internal amplification factor, β, is the lowering of the body factor, because $C_{ox} < 0; |C_{ox}| > C_s$ in NCFET and body factor "m" followed by Eq. (27), which directly influence the SS

$$m = \frac{1}{\beta} \times \frac{\partial V_{int}}{\partial \psi_s} = \frac{1}{\beta} \times \left(1 + \frac{C_S}{C_{ox}}\right) \ll 1 \tag{27}$$

For NC FET technology, using the amplification factor, $\beta > 1$, the SS of an NCFET is defined by,

$$SS_{nc} = \left(\frac{\partial \log I_{DS}}{\partial V_{gs}}\right)^{-1} = \frac{\partial V_{int}}{\partial \log I_{DS}} \times \frac{\partial V_{gs}}{V_{int}} = \frac{SS_{Bulk}}{\beta} \tag{28}$$

It is known that for NCFET, $\beta > 1$ and the $SS_{NC} > SS_{Bulk}$. As shown in Eq. (27), the concept of negative capacitance, in the conventional transistor gate stack achieves steep SS through the NC voltage amplification effect by adding a ferroelectric layer.

Currently semiconductor device developers have proposed and developed various type of FET devices by implementing the concept of negative capacitance known as metal ferroelectric semiconductor field-effect transistor (MFSFET), metal ferroelectric insulator semiconductor field-effect transistor (MFISFET), and metal ferroelectric metal insulator semiconductor field-effect transistor (MFMISFET). However, the basic operation principle in NCFET is to realize a match between the channel charge (Q_{CH}) and the ferroelectric polarization charge $\overrightarrow{P}$, irrespective of specific gate structure is used.

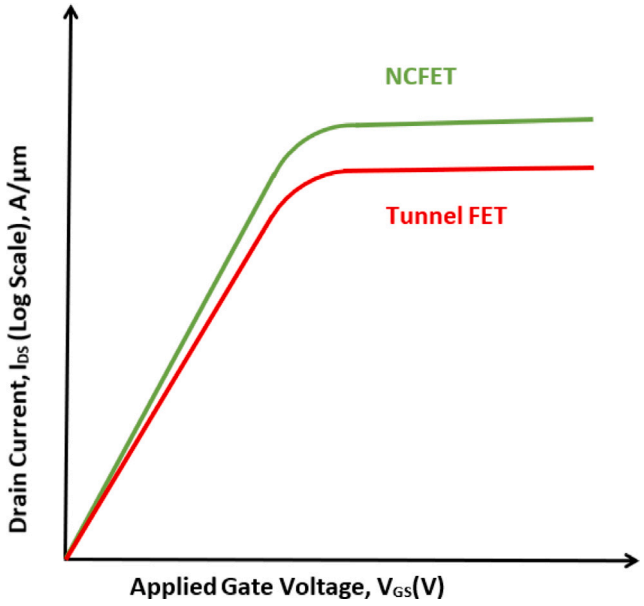

Fig. 11. Transfer characteristics of conventional NCFET versus Tunnel FET.

From Tables 2 and 4, it has been observed that at same operating condition, NCFET shows higher I_{ON} than Tunnel FETs. Lower I_{OFF} in NCFET helps to reduce the power dissipation and higher I_{ON} shows

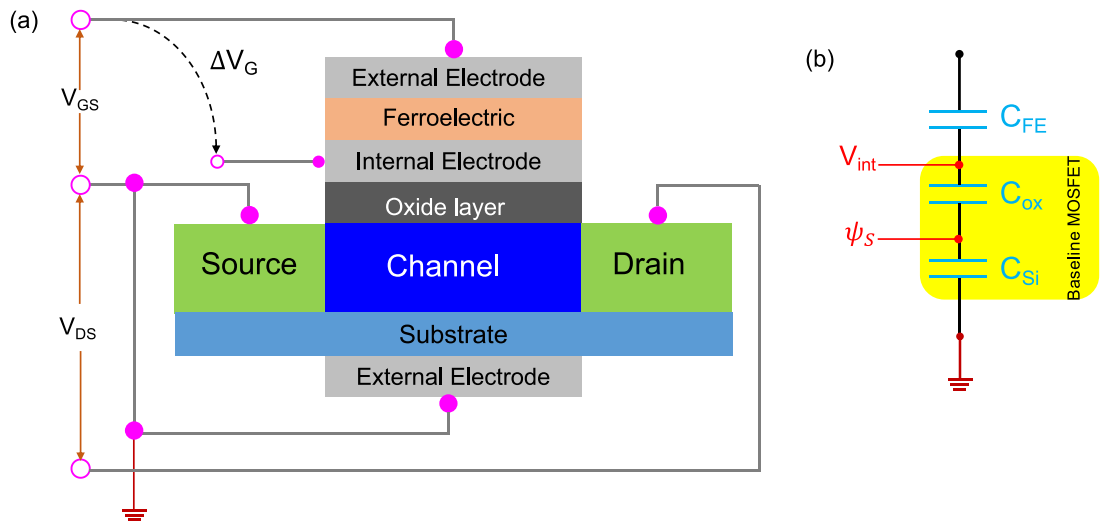

Fig. 12. (a) Schematic diagram of NCFET, (b) capacitance model.

better switching behavior, this indicates improved g_m than Tunnel FET. The steep SS values proved lowering supply voltage i.e., further scaling of supply voltage. Table 5, has reported available latest undated in NC Tunnel FET. Published report shows an improvement in NC TFET at similar operating situation and convention TFET.

6. Current–voltage characteristics of NCFET

This section is a brief discussion on I–V characteristic of NCFET device for investigation of device operation purpose. The I–V analysis based on following section shown in schematic, Fig. 12(a) [88,89]. Fig. 12(b) is equivalent capacitance model of NCFET is shown in Fig. 12(a). As shown in capacitance model, the voltage inside NCFET device is noted V_{int}. The surface potential is denoted as ψ_S and voltage at gate node is V_{gs}. The capacitances in this model are noted as C_S, C_{FE} and C_{ox}. for channel to source/drain, FE layer and used oxide in device respectively.

The dynamics of C_{FE} is included with the L–K equation with Gibb's free energy model have been used in Eq. (29). Now V_{FE} can be modeled as:

$$V_{FE} = 2\alpha T_{FE} P + 4\beta T_{FE} P^3 + 6\gamma T_{FE} P^5 + \rho T_{FE} \frac{dP}{dt} \tag{29}$$

By using energy conservation principle, V_{gs} for device shown in Fig. 12(b), the potential balance equation can be written as:

$$V_{gs} = V_{FE} + V_{FB} + \psi_S + V_{ox} \tag{30}$$

As shown in Fig. 12(a), ΔV_G is change in gate voltage due to added FE materials. The change in external gate voltage depends on T_{FE} and material property known as Landau coefficient (α, β, γ). In Eq. (30), V_{FE} is potential across FE, V_{FB} is flat band voltage, ψ_S surface potential, V_{ox} is the voltage drop across used dielectric material. In Eq. (29) are the potential across the oxide layer and the flat-band voltage with the Poisson's equation is used, leading to following Eq. (31).

$$V_{gs} = V_{int}\left[1 + \frac{1}{2} V_{int}\left(\frac{dC_{MOS}}{dQ}\right)\right] + T_{FE}\left[2\alpha\left(\frac{Q}{A}\right) + 4\beta\left(\frac{Q}{A}\right)^3 + 6\gamma\left(\frac{Q}{A}\right)^5\right] \tag{31}$$

where, V_{int} is written as

$$V_{int} = V_{FB} + \psi_s + \frac{\sqrt{2\epsilon_{Si} k_B T N_A}}{C_{ox}} \sqrt{\frac{q\psi_s}{k_B T} + \frac{n_i^2}{N_A^2} e^{q(\psi_s - (V+\psi_0))/k_B T}} \tag{32}$$

In NCFET device operation, $Q_S = Q_i + Q_d$, here Q_i and Q_d is popularly known as inversion charge and depletion charge density respectively. Now $Q_i = Q_S - Q_d$ as

$$Q_i = -2\sqrt{2\epsilon_{Si} k_B T N_A} \times \sqrt{\frac{q\psi_s}{k_B T} + \frac{n_i^2}{N_A^2} e^{q(\psi_s - (V+\psi_0))/k_B T}} + 2\sqrt{2\epsilon_{Si} q N_A \psi_s} \tag{33}$$

Now drain current in NCFET can be modeled by Eq. (33).

$$I_{DS} = \mu_{eff} \frac{W}{L} \int_{V_S}^{V_D} [-Q_i(V)] dV \tag{34}$$

where, μ_{eff} is the effective mobility having drift and diffusion component, V_S and V_D are potential at source and drain terminal, and W and L are channel width and length, respectively. By substituting, the value Q_i from Eq. (33) in Eq. (34), we can obtain an expression governing for drain current of NCFET. The qualitative I–V characteristic for NCFET is shown in Fig. 13. The NCFET devices have achieved same I_{ON} at lower supply voltage as compared to conventional MOSFET without compromise with I_{OFF}. This indicates that NCFET based circuit and system consume less power without any loss in speed.

7. Impact of negative capacitance on circuit design

For subthreshold operation regime, subthreshold slope is ratio of change in drain current (ΔI_{DS}) with applied gate voltage (ΔV_{gs}) respectively, followed by tangent rule. For conventional MOSFET, where drain current is plotted on y-axis in log scale and input voltage of device, V_{gs} on x-axis, shown in Fig. 14.

$$\begin{aligned} Subthreshold\ Slope &= \frac{\Delta \log_{10} I_{DS}}{\Delta V_{gs}} \\ &= \frac{1}{\log(10)} \times \frac{\partial I_{DS}}{\partial V_{gs}} \\ &= \frac{1}{\log(10)} \times g_m \end{aligned} \tag{35}$$

Since SS is inverse of defined slope in Eq. (35) [90,91]. Now Eq. (35), can be written as [75]

$$\frac{g_m}{I_{D_S}} = \frac{\log(10)}{SS} \tag{35.1}$$

The g_m/I_{DS} ratio is also known as "transconductance generation ratio", an important circuit design parameter for low power circuits. The mathematical Eq. (36), indicates the future scope for achieving

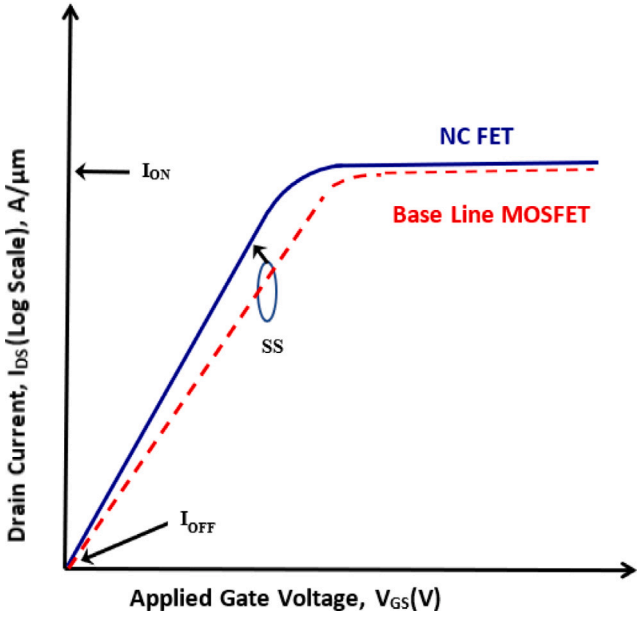

Fig. 13. I–V characteristics of negative capacitance field-effect transistor.

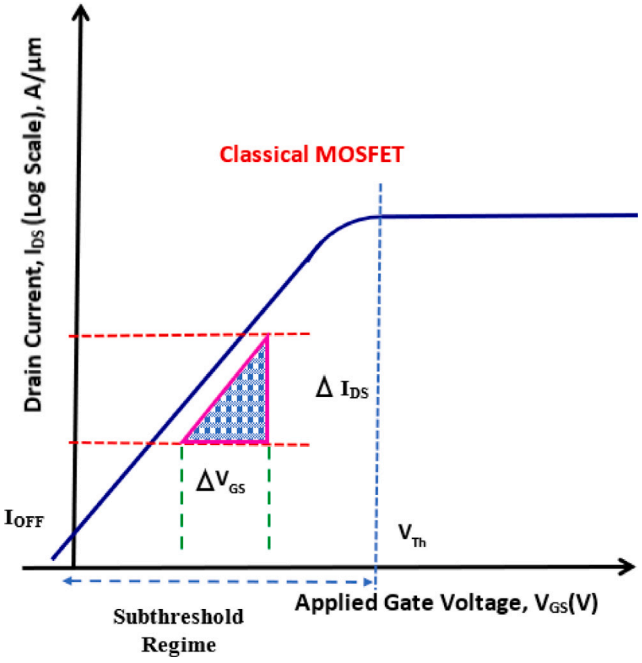

Fig. 14. Transfer characteristic of MOSFET.

higher g_m/I_{DS} value than conventional MOSFET, due to lower SS with popular SS FET devices such as TFET and NCFET devices.

By using Eq. (35), for classical MOSFET, which have 60 mV/$decade$ SS value, maximum $(g_m/I_{DS})_{MOSFET} \sim 38.5V^{-1}$

$$\left(\frac{g_m}{I_{DS}}\right)_{MOSFET} = \frac{\log(10)}{SS_{MOSFET}} \tag{36}$$

NCFET is follow the similar current transport drift diffusion model, only slight modification of gate control region containing thin layer of FE layer. Due this we have adopted the conventional subthreshold analysis model for NCFET here. Now for NCFET,

$$\left(\frac{g_m}{I_{DS}}\right)_{NCFET} = \frac{\log(10)}{SS_{NCFET}} \tag{37}$$

By using Eqs. (37) and (38), we have following relation,

$$\frac{\left(\frac{g_m}{I_{DS}}\right)_{NCFET}}{\left(\frac{g_m}{I_{DS}}\right)_{MOSFET}} = \frac{SS_{MOSFET}}{SS_{NCFET}} \tag{38}$$

Now Eq. (39), becomes

$$\frac{\left(\frac{g_m}{I_{DS}}\right)_{NCFET}}{\left(\frac{g_m}{I_{DS}}\right)_{MOSFET}} = \frac{60\ \text{mV}/decade|T = 300\ \text{K}}{SS_{NCFET}} \tag{38.1}$$

The reported evidence about NCFET shows that $SS_{NCFET} < 60$ mV/$decade$, thus the numeric value of Eq. (39) is always greater than 1, i.e.

$$\frac{\left(\frac{g_m}{I_{DS}}\right)_{NCFET}}{\left(\frac{g_m}{I_{DS}}\right)_{MOSFET}} > 1 \tag{39}$$

The larger g_m, lower SS, and $(g_m/I_{DS})_{NCFET} > (g_m/I_{DS})_{MOSFET}$ indicates NCFET has capability to overcome the limitation of conventional MOSFET technology and helpful for development of newly proposed low power circuit and system.

In circuit design, for certain gain bandwidth GBW design targets, an excellent g_m/I_{DS} is required. This is for minimum circuit current consumption. On the basic of conceptual circuit design analysis and Eq. (38), indicate that NCFET having optimum g_m/I_{DS} value than conventional MOSFET and its competitor Tunnel FETs. For a power efficient technology, this analysis indicates that $(g_m/I_{DS})_{max}$ is also required.

The power factor of designed circuit can be optimized by adoption the NCFET devices, due to lowered power supply device. The square dependency with supply voltage (i.e., $P_{switching} \propto \alpha C V_{DD}^2$), but total capacitance in NCFET (i.e., $C_{NCFET} = C_{FE} \times C_{BaseMOS}/((C_{FE}+C_{BaseMOS})) > C_{BaseMOS}$). In case of NCFET, gate capacitance C_{gg} is always larger than conventional MOSFET. This indicated that when circuit is implemented by NCFET technology will consume higher switching power as compared to conventional CMOS. Energy per switching estimated by $E \propto V_{DD}^2(\epsilon + I_{OFF}/I_{ON})$ in case of NCFET devices also lower as compared to conventional CMOS.

Further, many NC-FET based analog circuits have been investigated by the researchers. Linag et al. [92] in 2018 investigated the NC-FET based sample and hold circuit. The performance of Analog to digital converter (ADC) and phase-looked-loop (PLL) have been boosted by using NCFET [93]. Moreover, the drain induced barrier lowering (DIBL) is an important parameter measure for circuity performance analysis of device in conventional CMOS technology. In conventional CMOS Technology, DIBL increases with V_{DD} scaling, causes increment in SCEs. While in rigorous investigation of NCFET, it is found that DIBL reduces with V_{DD} scaling, an indication of reduction in SCEs, that in turn improve the circuit performance [85,92–95].

8. Conclusion

It has been remarked that, the increasing power dissipation and thermal management issues of high-volume ICs and system can be addressed by the evolution of steep-slope devices. This is possible only due to SS devices because these devices always switch on low supply voltage, which help to reduce the power consumption of device. In modern era, TFET and NCFET are found two most suitable FET device, which have steep subthreshold slope feature. Due to lower I_{ON} in TFET, and NCFETs have upper hand over the TFET. In this review paper, the impacts of NC due to FE materials have been investigated. The NCFET technology, the ICs can still meet the same performance as the conventional CMOS devices, at lower V_{DD}. This leads to a significant power saving high-performance, high volume applications. Unlike TFET, NCFET technology does not alter, the carrier transport physics of devices. This feature of NCFETs reduces the development

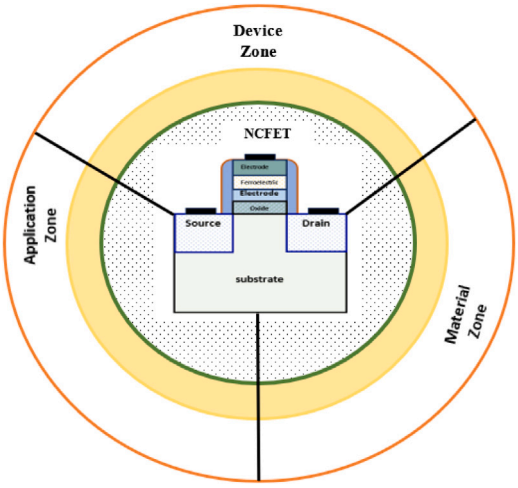

Fig. 15. Impact and development scope.

cost ongoing research for improvement of MOS carrier transport. The development of NCFET technology and related devices have sufficient design domain and opportunities for development of conventional and non-conventional ultra-low power circuit and system for mankind.

9. Future scope

Fig. 15 shows the impact and future scope of NCFET device. Intuitionally the development scope has been presented via Y-shaped graph. The development of NC concept has full scope of development in device, circuit and system sector shown in Y-shaped graph. The development of NC opens door in materials science engineering and technology for further improvement, classified in Y-chart known as material zone.

Various FET device architecture have been proposed and developed for implementing NC concept, this sector in Y-chart known as device zone. Third zone of Y-chart is known as applications. The available research articles approved that NCFET having improved FET features than conventional CMOS technology specially for ultra-low power sector. Expectation of revolution in circuit and system sector is expected with NCFET. The observation of Y-shaped progress and development chart advocated the invention of NCFET re-opens the door for research and development in materials science engineering, new circuit and system based on NCFET for ultra-low power applications.

NCFET is one of the promising emerging technologies have capabilities overcome the fundamental limits of conventional CMOS technology. NCFET are meant to maintain the performance while reducing power computation and switching energy. As per available scientific information about semiconductor device technology, it can be recommended that, NCFET technology can bypass the limitation of present CMOS technology and will play a leading role for future development. This device technology has full design scope and capability to reduce the product and production cost of highly sophisticated system like portable system and IoTs.

CRediT authorship contribution statement

Shiromani Balmukund Rahi: Conceptualization, Methodology, Writing - original draft. **Shubham Tayal:** Formal analysis, Resources, Data curation, Writing - review & editing. **Abhishek Kumar Upadhyay:** Software, Validation, Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] N. Chowdhury, S.F. Azad, Q.D. Khosru, Negative capacitance tunnel field effect transistor: A novel device with low subthreshold swing and high on current, ECS Trans. 58 (16) (2014) 1.

[2] W. You, P. Su, Design space exploration considering back-gate biasing effects for 2D negative-capacitance field-effect transistors, IEEE Trans. Electron Devices 64 (8) (2017) 3476–3481.

[3] D. Jimenez, E. Miranda, A. Godoy, Analytic model for the surface potential and drain current in negative capacitance field-effect transistors, IEEE Trans. Electron Devices 57 (10) (2010) 2405–2409.

[4] C. Jiang, R. Liang, J. Xu, Investigation of negative capacitance gate-all-around tunnel FETs combining numerical simulation and analytical modeling, IEEE Trans. Nanotechnol. 16 (1) (2017) 58–67.

[5] T. Yu, W. Lü, Z. Zhao, P. Si, K. Zhang, Effect of different capacitance matching on negative capacitance FDSOI transistors, Microelectron. J. 98 (Apr.) (2020) 104730.

[6] Jaesung Jo, Woo Young Choi, Jung-Dongand Park, Jae Won Shim, Hyun-Yong Yu, Shin, Negative capacitance in organic/ferroelectric capacitor to implement steep switching MOS devices, Nano Lett. 15 (7) (2015) 4553–4556.

[7] W. You, P. Su, Design space exploration considering back-gate biasing effects for 2D negative-capacitance field-effect transistors, IEEE Trans. Electron Devices 64 (8) (2017) 3476–3481.

[8] Y.H. Liao, et al., Electric field-induced permittivity enhancement in negative-capacitance FET, IEEE Trans. Electron Devices 68 (3) (2021) 1346–1351.

[9] H. Ota, S. Migita, J. Hattori, K. Fukuda, A. Torikumi, Structural advantages of silicon-on-insulator FETs over FinFETs in steep subthreshold-swing operation in ferroelectric-gate FETs, Japan. J. Appl. Phys. 56 (4) (2017).

[10] S. Dasgupta, et al., Sub-kT/q Switching in Strong Inversion in PbZr0.52Ti0.48O3 Gated Negative Capacitance FETs, IEEE J. Explor. Solid-State Comput. Devices Circuits 1 (Dec.) (2015) 43–48.

[11] H. Ota, S. Migita, J. Hattori, K. Fukuda, A. Toriumi, Material and device engineering in fully depleted silicon-on-insulator transistors to realize a steep subthreshold swing using negative capacitance, Japan. J. Appl. Phys. 55 (Apr.) (2016).

[12] Y. Li, K. Yao, G.S. Samudra, Effect of ferroelectric damping on dynamic characteristics of negative capacitance ferroelectric MOSFET, IEEE Trans. Electron Devices 63 (9) (2016) 3636–3641.

[13] Y. Li, Y. Kang, X. Gong, Evaluation of negative capacitance ferroelectric MOSFET for analog circuit applications, IEEE Trans. Electron Devices 64 (10) (2017) 4317–4321.

[14] C.W. Yeung, A.I. Khan, A. Sarkar, S. Salahuddin, C. Hu, Low power negative capacitance FETs for future quantum-well body technology, in: 2013 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2013, pp. 1–2.

[15] Daniel Appleby, Nikhil K. Ponon, Kelvin S.K. Kwa, Bin Zou, Peter K. Petrov, Tianle Wang, Neil M. Alford, Anthony O. Neill, Experimental observation of negative capacitance in ferroelectrics at room temperature, Nano Lett. 14 (7) (2014) 3864–3868.

[16] A.I. Khan, U. Radhakrishna, S. Salahuddin, D. Antoniadis, Work function engineering for performance improvement in leaky negative capacitance FETs, IEEE Electron Device Lett. 38 (9) (2017) 1335–1338.

[17] H. Ilatikhameneh, T.A. Ameen, C. Chen, G. Klimeck, R. Rahman, Sensitivity challenge of steep transistors, IEEE Trans. Electron Devices 65 (4) (2018) 1633–1639.

[18] A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy efficient electronic switches, Nature 479 (7373) (2011) 329–337.

[19] N. Guenifi, S.B. Rahi, Design and optimization of tunnel fet based circuit parameters for low power integrated system and impact of thermal sensitivity, April 2021 Silicon.

[20] S.B. Rahi, P. Asthana, S. Gupta, Heterogate junctionless tunnel field-effect transistor: future of low-power devices, J. Comput. Electron. 16 (1) (2017) 30–38.

[21] P.K. Asthana, B. Ghosh, S.B. Rahi, Y. Goswami, Optimal design of high performance H-JLTFET using HfO2 as gate dielectric for ultra-low power applications, RSC Adv. 4 (43) (2014) 22803–22807.

[22] C. Jiang, L. Zhong, L. Xie, Impact of interface trap charges on the electrical characteristics of back-gated 2D negative capacitance (NC) FET, IEEE Trans. Nanotechnol. 18 (2019) 1204–1207.

[23] N. Bagga, N. Chauhan, A. Bulusu, S. Dasgupta, Demonstration of a novel ferroelectric-dielectric negative capacitance tunnel FET, in: 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), 2019, pp. 102–105.

[24] Huimin. Wang, et al., New insights into the physical origin of negative capacitance and hysteresis in NCFETs, in: IEDM, S31-1, Dec. 2018.

[25] T.N. Theis, P.M. Solomon, In quest of the next switch: Prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor, Proc. IEEE 98 (12) (2010) 2005–2014.

[26] Q. Huang, et al., A Novel Si Tunnel FET with 36mV/Dec Subthreshold Slope Based on Junction Depleted-Modulation Through Striped Gate Configuration, IEDM, 2012, pp. 187–190.

[27] E. Memisevic, et al., Vertical InAs/GaAsSb/ GaSb tunneling field-effect transistor on Si with S=48 MV/Decade and $I_{on} = 10\mu a/\mu M$ for $I_{Off} = 1NA/\mu M$ At $V_{DS} = 0.3V$, in: IEDM, Dec. 2016, pp. 500–503.

[28] M. Hoffmann, S. Slesazeck, T. Mikolajick, Progress and future prospects of negative capacitance electronics: A materials perspective, APL Mater. 9 (2) (2021) 020902.

[29] A.K. Saha, S. Datta and. S. K. Gupta, Negative capacitance in resistor-ferroelectric and ferroelectric-dielectric networks: Apparent or intrinsic? J. Appl. Phys., 123(10), 1051022018.

[30] L.D. Landau, I.M. Khalatnikov, On the anomalous absorption of sound near a second order phase transition point, Dokl. Akad. Nauk SSSR 96 (1954) 469–472.

[31] T.K. Song, Landau-Khalatnikov simulations for ferroelectric switching in ferroelectric random access memory application, J. Korean Phys. Soc. 46 (1) (2005) 5.

[32] M. Soleimani, N. Asoudegi, P. Khakbaz, M. Pourfath, Negative capacitance field-effect transistor based on a two-dimensional ferroelectric, in: 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2019, pp. 1–4.

[33] C.W. Yeung, A.I. Khan, A. Sarker, S. Salahuddin, C. Hu, Low power negative capacitance FETs for future quantum-well body technology, in: 2013 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2013, pp. 1–2.

[34] Y.G. Xiao, M.H. Tang, Y. Xiong, J.C. Li, C.P. Cheng, B. Jiang, Y.C. Zhou, Use of negative capacitance to simulate the electrical characteristics in double-gate ferroelectric field-effect transistors, Curr. Appl. Phys. 12 (6) (2012) 1591–1595.

[35] A.I. Khan, C.W. Yeung, C. Hu, S. Salahuddin, Ferroelectricnegative capacitance MOSFET: capacitance tuning & antiferroelectric operation, in: Electron Devices Meeting (IEDM), 2011 IEEE International, IEEE, 2011.

[36] Q. Huang, et al., First foundry platform of complementary Tunnel-FETs in CMOS baseline technology for ultralow-power IoT applications: Manufacturability, Variability and Technology Roadmap, in: IEDM, Dec. 2015, pp. 604–607.

[37] M. Nadeem, I. Di Bernardo, X. Wang, M. Fuhrer, D. Culcer, Overcoming Boltzmann's tyranny in a transistor via the topological quantum field effect, Nano Lett. 21 (7) (2021) 3155–3161.

[38] R. Dutta, T.D. Subash, N. Paitya, Improved DC performance analysis of a novel asymmetric extended source tunnel FET (AES-TFET) for fast switching application, Silicon (2021) 1–7.

[39] L. Lattanzio, L. De Michielis, A.M. Ionescu, Complementary germanium electron–hole bilayer tunnel FET for sub-0.5-V operation, IEEE Electron Device Lett. 33 (2) (2012) 167–169.

[40] D. Esseni, M. Alioto, Device-circuit co-design and comparison of ultra-low voltage Tunnel-FET and CMOS digital circuits, in: 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), 2014, pp. 321–324.

[41] S. Bala, M. Khosla, Design and simulation of nanoscale double-gate TFET/tunnel CNTFET, J. Semicond. 39 (4) (2018) 044001.

[42] A. Saeidi, et al., Negative capacitance as performance booster for tunnel FETs and MOSFETs: An experimental study, IEEE Electron Device Lett. 38 (10) (2017) 1485–1488.

[43] A.M. Ionescu, L. De Michielis, N. Dagtekin, G. Salvatore, J. Cao, A. Rusu, S. Bartsch, Ultra low power: Emerging devices and their benefits for integrated circuits, in: Electron Devices Meeting (IEDM), 2011 IEEE International, IEEE, 2011.

[44] S. Salahuddin, S. Datta, Use of negative capacitance to provide voltage amplification for low power nanoscale devices, Nano Lett. 8 (2) (2008) 405–410.

[45] S. Salahuddin, Review of negative capacitance transistors, in: 2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2016, pp. 1–1.

[46] Z. Dong, J. Guo, A simple model of negative capacitance FET with electrostatic short channel effects, IEEE Trans. Electron Devices 64 (7) (2017) 2927–2934.

[47] B. Obradovic, et al., Ferroelectric switching delay as cause of negative capacitance and the implication to NCFETs, in: VLSI, Jun. 2018, p. 51–52.

[48] C. Lin, A.I. Khan, S. Salahuddin, C. Hu, Effects of the variation of ferroelectric properties on negative capacitance FET characteristics, IEEE Trans. Electron Devices 63 (5) (2016) 2197–2199.

[49] A.I. Khan, et al., Negative capacitance in a ferroelectric capacitor, Nature Mater. 14 (2) (2015) 182–186.

[50] D.J. Appleby, N.K. Ponon, K.S. Kwa, B. Zou, P.K. Petrov, T. Wang, N.M. Alford, A.O. Neill, Experimental observation of negative capacitance in ferroelectrics at room temperature, Nano Lett. 14 (7) (2014) 3864–3868.

[51] A. Rusu, A. Saeidi, A.M. Ionescu, Condition for the negative capacitance effect in metal–ferroelectric–insulator–semiconductor devices, Nanotechnology 27 (11) (2016) 115201.

[52] A. Saeidi, F. Jazaeri, I. Stolichnov, A.M. Ionescu, Double-gate negative-capacitance MOSFET with PZT gate-stack on ultra-thin body SOI: An experimentally calibrated simulation study of device performance, IEEE Trans. Electron Devices 63 (12) (2016) 4678–4684.

[53] J. Lee, C. Choi, B. Park, T. Noh, J. Lee, Built-in voltages and asymmetric polarization switching in Pb (Zr, Ti) O3 thin film capacitors, Appl. Phys. Lett. 72 (25) (1998) 3380–3382.

[54] A. Saeidi, A. Biswas, A.M. Ionescu, Modeling and simulation of low power ferroelectric non-volatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric, Solid-State Electron. 124 (2016) 16–23.

[55] A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy efficient electronic switches, Nature 479 (7373) (2011) 329–337.

[56] C. Wu, R. Huang, Q. Huang, C. Wang, J. Wang, Y. Wang, An analytical surface potential model accounting for the dual-modulation effects in tunnel FETs, IEEE Trans. Electron Devices 61 (8) (2014) 2690–2696.

[57] A. Rusu, G.A. Salvatore, D. Jimenez, A.M. Ionescu, Metalferroelectric-metal–oxide–semiconductor field effect transistor with sub- 60mv/decade subthreshold swing and internal voltage amplification, in: Electron Devices Meeting (IEDM), 2010 IEEE International, IEEE, 2010.

[58] J. Jo, W.Y. Choi, J.-D. Park, J.W. Shim, H.-Y. Yu, C. Shin, Negative capacitance in organic/ferroelectric capacitor to implement steep switching MOS devices, Nano Lett. 15 (7) (2015) 4553–4556.

[59] M. Kobayashi, C. Jin, T. Hiramoto, Comprehensive understanding of negative capacitance FET from the perspective of transient ferroelectric model, in: 2019 IEEE 13th International Conference on ASIC (ASICON), 2019, pp. 1–4.

[60] M.H. Lee, et al., Ferroelectric negative capacitance hetero-tunnel field-effect-transistors with internal voltage amplification, in: 2013 IEEE International Electron Devices Meeting, 2013, pp. 4.5.1–4.5.4.

[61] H. Lin, V.P. Hu, Device designs and analog performance analysis for negative-capacitance vertical-tunnel FET, in: 20th International Symposium on Quality Electronic Design (ISQED), 2019, pp. 241–246.

[62] Y. Zhao, et al., Experimental study on the transient response of negative capacitance tunnel FET, in: 2019 Electron Devices Technology and Manufacturing Conference (EDTM), 2019, pp. 88–90.

[63] V.P. Hu, H. Lin, Y. Lin, C. Hu, Optimization of negative-capacitance vertical-tunnel FET (NCVT-FET), IEEE Trans. Electron Devices 67 (6) (2020) 2593–2599.

[64] M. Kobayashi, K. Jang, N. Ueyama, T. Hiramoto, Negative capacitance for boosting tunnel FET performance, IEEE Trans. Nanotechnol. 16 (2) (2017) 253–258.

[65] A. Saeidi, et al., Near hysteresis-free negative capacitance InGaAs tunnel FETs with enhanced digital and analog figures of merit below =400 mV, in: 2018 IEEE International Electron Devices Meeting (IEDM), 2018, pp. 13.4.1–13.4.4.

[66] M. Kumar, S. Jit, A novel four-terminal ferroelectric tunnel FET for quasi-ideal switch, IEEE Trans. Nanotechnol. 14 (4) (2015) 600–602.

[67] Seabaugh, et al., Steep slope transistors: Tunnel FETs and beyond, in: 2016 46th European Solid-State Device Research Conference (ESSDERC), 2016, pp. 349–351.

[68] S. Singh, P. Pal, R. Mittal, A. Tamia, P.N. Kondekar, Silicon on ferroelectric Tunnel FET (SOF-TFET) for low power application, in: 2014 IEEE 2nd International Conference on Emerging Electronics (ICEE), 2014, pp. 1–3.

[69] M.H. Lee, et al., Ferroelectric negative capacitance hetero-tunnel field-effect-transistors with internal voltage amplification, in: 2013 IEEE International Electron Devices Meeting, 2013, pp. 4.5.1–4.5.4.

[70] Saeidi, et al., Negative capacitance as performance booster for tunnel FETs and MOSFETs: An experimental study, IEEE Electron Device Lett. 38 (10) (2017) 1485–1488.

[71] S. Guo, R.J. Prentki, K. Jin, C. l. Chen, H. Guo, Negative-capacitance FET with a cold source, IEEE Trans. Electron Devices 68 (2) (2021) 911–918.

[72] Masaharu. Kobayashi, et al., Experimental study om polazrization-limited operation speed of negative capacitance FET with ferroelectric HfO2, in: IEDM, Dec. 2016, pp. 314–317.

[73] L. Barboni, M. Siniscalchi, B. Sensale-Rodriguez, TFET-Based circuit design using the transconductance generation efficiency g_m/I_d method, IEEE J. Electron Devices Soc. 3 (3) (2015) 208–216, http://dx.doi.org/10.1109/JEDS.2015.2412118.

[74] M.-Y. Kao, S. Salahuddin, C. Hu, Negative capacitance enables GAA scaling VDD to 0.5 V, Solid-State Electron. 181–182 (Aug.) (2021) 108010.

[75] H. Zhou, M. Zhang, D. Le, Y. Hao, Challenges from quantum capacitance in process of high-performance carbon nanotube-FETs design, in: 2010 2nd International Conference on Computer Engineering and Technology, 2010, pp. V3-256–V3-259.

[76] H.W. Kim, D. Kwon, Gate-normal negative capacitance tunnel field-effect transistor (TFET) with channel doping engineering, IEEE Trans. Nanotechnol. 20 (2021) 278–281.
[77] R.N. Sajjad, D. Antoniadis, A compact model for tunnel FET for all operation regimes including trap assisted tunneling, in: 2016 74th Annual Device Research Conference (DRC), 2016, pp. 1–2.
[78] Y. Zhao, et al., A novel negative capacitance tunnel FET with improved subthreshold swing and nearly non-hysteresis through hybrid modulation, IEEE Electron Device Lett. 40 (6) (2019) 989–992.
[79] Jain, M.A. Alam, Proposal of a hysteresis-free zero subthreshold swing field-effect transistor, IEEE Trans. Electron Devices 61 (10) (2014) 3546–3552.
[80] M. Kobayashi, K. Jang, N. Ueyama, T. Hiramoto, Negative capacitance as a performance booster for tunnel FET, in: 2016 IEEE Silicon Nanoelectronics Workshop (SNW), 2016, pp. 150–151.
[81] C. Su, Q. Huang, M. Yang, L. Chen, Z. Liang, R. Huang, Origin of steep subthreshold swing within the low drain current range in negative capacitance field effect transistor, in: 2020 China Semiconductor Technology International Conference (CSTIC), 2020, pp. 1–3.
[82] M.H. Lee, C. Kao, C.Yang, C. Lee, P-type tunneling FET on Si (110) substrate with anisotropic effect, in: 69th Device Research Conference, 2011, pp. 207–208.
[83] Y.H. Liao, et al., Electric field-induced permittivity enhancement in negative-capacitance FET, IEEE Trans. Electron Devices 68 (3) (2021) 1346–1351.
[84] M. Kobayashi, C. Jin, T. Hiramoto, Comprehensive understanding of negative capacitance FET from the perspective of transient ferroelectric model, in: 2019 IEEE 13th International Conference on ASIC (ASICON), 2019, pp. 1–4.
[85] Y. Liang, Z. Zhu, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Mismatch of ferroelectric film on negative capacitance FETs performance, IEEE Trans. Electron Devices 67 (3) (2020) 1297–1304, http://dx.doi.org/10.1109/TED.2020.2968050.
[86] H. Lee, Y. Yoon, C. Shin, Current-voltage model for negative capacitance field-effect transistors, IEEE Electron Device Lett. 38 (5) (2017) 669–672.
[87] Y. Taur, T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge Univ. Press, Cambridge, U.K., 1998.
[88] A.R. Trivedi, S. Carlo, S. Mukhopadhyay, Exploring Tunnel-FET for ultra-low power analog applications: A case study on operational transconductance amplifier, in: 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC), 2013, pp. 1–6.
[89] B. Sedighi, X.S. Hu, H. Liu, J.J. Nahas, M. Niemier, Analog circuit design using tunnel-FETs, IEEE Trans. Circuits Syst. I. Regul. Pap. 62 (1) (2015) 39–48.
[90] T. Yu, W. Lu, Z. Zao, P. Si, K. Zhang, Effect of different capacitance matching on negative capacitance FDSOI transistors, Microelectron. J. 98 (Apr.) (2020) 104730.
[91] T. Yu, W. Lü, Z. Zhao, P. Si, K. Zhang, Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors, Microelectron. J. 108 (Feb.) (2021) 104981.
[92] Y. Liang, et al., Influence of body effect on sample-and-hold circuit design using negative capacitance FET, IEEE Trans. Electron Devices 65 (9) (2018) 3909–3914, http://dx.doi.org/10.1109/TED.2018.2852679.
[93] Y. Liang, Z. Zhu, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Utilization of negative-capacitance FETs to boost analog circuit performances, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 27 (12) (2019) 2855–2860, http://dx.doi.org/10.1109/TVLSI.2019.2932268.
[94] Y. Liang, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Analysis of DIBL effect and negative resistance performance for NCFET based on a compact SPICE model, IEEE Trans. Electron Devices 65 (12) (2018) 5525–5529, http://dx.doi.org/10.1109/TED.2018.2875661.
[95] Tianyu Yu, Weifeng Lü, Zhifeng Zhao, Peng Si, Zhang Kai, Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors, Microelectron. J. 108 (2021) http://dx.doi.org/10.1016/j.mejo.2020.104981.