Investigation of Analog Parameters and Miller Capacitance Affecting the Circuit Performance of Double Gate Tunnel Field Effect Transistors

Deepak Kumar, Shiromani Balmukund Rahi, and Piyush Kuchhal

Abstract TCAD Simulations for 30 nm double gate tunnel field effect transistor (DGTFET) reports steeper subthreshold swing, SS ~ 15 mV/dec, I_{ON} ~ 10^{-4} A/μm, and low off-state current I_{OFF} ~ 10^{-15}A/μm as desirable parameters for low voltage applications. The unity gain frequency (f_T) increases with V_{gs} and maximizes at 5.2 × 10^{11} Hz for $V_{gs} = V_{ds} = 0.7$ V. It is investigated that the gain-bandwidth product (GBP) also increase with Vgs and maximized at 2.63 × 10^{11} Hz for $V_{ds} = 0.7$ V at $V_{gs} = 0.6$ V. Transconductance frequency product (TFP) increases initially with V_{gs} (0–0.7 V) and maximizes at 4.46 × 10^{11} Hz/V for $V_{ds} = 0.7$ V. Higher value of V_{ds} results in better response time of the DGTFETs, i.e., increasing V_{ds} from 0.1 to 0.8 V, the transit time (t_r) of the electron decreases from 4 to 0.1 ps resulting faster switching operation. Transient performance of DGTFETs reports that at supply voltage (V_{DD}) = 0.7 V, increasing the load capacitance (C_L, 10–200 pF) the total delay increases from 0.18 to 1.9 ns. It is also noticed that the % peak voltage overshoot (% V_p) decreases from 42.8 to 2.14% due to decrease in computed values of miller capacitance (C_{MIL}) from 11.27 to 4.32 fF. Maintaining $C_L = 15$ fF, increasing V_{DD} reports significant variation in voltage peak overshoot from 35 to 26.25% and total delay also decreases from 8 to 0.2 ns for $V_{DD} = 0.1$–0.8 V.

Keywords Band-to-band tunneling (BTBT) · Analog · Transient · TFET · Miller capacitance · Verilog A model · Symica D

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1 Introduction

The transistor density is continuously increasing with scaling conventional—MOSFETs which results in huge power dissipation inside integrated chips (ICs). The aggressive scaling of supply voltage (V_{DD}) for the CMOS devices which further reduces the dynamic power dissipation (~$C_L \times V_{DD}^2$) and same is low-power applications for advance technology nodes [1–4]. The threshold voltage (V_{th}) is needed to be scaled down proportionally as the supply voltage (V_{DD}) along with dimensional scaling to achieve sufficient on current (I_{ON}) in order to maintain satisfactory circuit and device performance. But Scaling down V_{th} further increases off-state current (I_{OFF}) significantly, hence increases static leakage power dissipation (~$V_{DD} \times I_{OFF}$) irrespective of scaled down V_{DD} and these impacts can be understood by the limitation of subthreshold swing (SS ~ 60 mV/decade) in MOSFETs due to conventional thermionic emission of electrons from source to channel. Therefore, it becomes essential to explore other structures of (FETs), those that have the potential to function at low supply voltage (V_{DD}), hence minimize the switching power. To meet these expectations, a new semiconductor device architecture based on quantum transport mechanism (QTM), called Tunneling Field Effect Transistor (TFET) is studied nowadays [5–16]. TFETs can be considered as a potential device structure for ultralow power applications due to their band-to-band (B2B) tunneling transport phenomenon [17–25]. Furthermore, the TFETs possess high-κ dielectric for deposition over the gate dimensions enhances the tunneling Electric field strength across junction formed across the body and the channel. Equation 1 shows that SS ($\partial V_{GS}/\partial \log I_{DS}$) of the TFET consist of different parameter as compared to a MOSFET [26–30].

$$SS = \ln\ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{E+b}{E^2}\frac{dE}{dV_{gs}}\right]^{-1} \tag{1}$$

The Eq. 1 shows that SS is not limited by kT/q; can achieve a steep SS for lower gate voltages as compared to MOSFETs. The electric field (E) across the source-channel junction is another key parameter to reduce the SS (< SS ~ 60 mV/dec) which further tends to reduce the subthreshold leakage power dissipation (E_L) in circuits as given by Eq. 2 [31, 32]. Due to its B2BT electron tunneling injection mechanism, a TFET has the potential to achieve lower SS particularly for low-power applications and have ability to cross the barrier of scaling limitations imposed by MOSFETs [30, 33–38].

$$E_L \propto V_{DD}^2 \cdot 10^{\frac{-V_{DD}}{SS}} \tag{2}$$

A 30 nm gate length double gate tunnel field effect transistor (DGFET) is simulated to achieve I–V and C–V characteristics in the Sentaurus 2D simulator. The features of the system are further used to evaluate the analog and transient (digital) output of DGTFETs by using Symica DE [39–45] to integrate a Verilog A model-based look-up table. The suitability of DGTFETs for analog applications is also studied by

comparing the analog output at different supply voltages (V_{DD}) of Double Gate (DG) n-channel TFETs. The analog parameters such as transconductance (g_m), gain bandwidth product (GBP), transit time (t_r), transconductance frequency product (TFP), and unity gain cut off frequency f_T [46] are also reported as Si DGTFET performance.

In DG TFET, the source and drain region's charges are coupled due to B2BT process leads to significant increase in Cgd induces of miller capacitance at drain's node. The higher miller capacitance (C_{MIL}) may have an impact on the peak voltage overshoots during transient performance [47, 48]. In order to analyze the effect of V_{DD} and load capacitance (C_L) on transient parameters and miller capacitance, digital simulations of DGTFETs based inverters are also reported.

2 Setup of Device Simulations for DGTFET

A DGTFET device structure is shown in Fig. 1 with the dimensions of the gate length $L_g = 30$ nm, body thickness $t_{si} = 7.0$ nm, gate oxide thickness $t_{ox} = 1.0$ nm; body dielectric $\varepsilon_{si} = 11.8\ \varepsilon_o$, oxide dielectric $\varepsilon_{ox} = 21.0\ \varepsilon_o$ (HfO_2). For NTFET, the source is uniformly doped with Boron (B) of 1.0×10^{20} cm^{-3}, doping of Phosphorus (P) of 1.0×10^{20} cm^{-3} is done at the drain region and B of 1.0×10^{16} cm^{-3} is doped in the channel region, respectively. Similarly for PTFET, the source is uniformly doped with P of 1.0×10^{20} cm^{-3}, doping of B of 1.0×10^{20} cm^{-3} is done at the drain region and B of 1.0×10^{16} cm^{-3} is doped in the channel region, respectively. TCAD simulations are performed in order to carry out the electrical characteristic (I–V/C–V) by considering dc and ac signal at 5 MHz) analysis. Non local B2BT model, Fermi statistics, SRH recombination, Poisson's, and continuity equations are coded in the simulation script to achieve device simulation [49]. Simulations also considered gate metal work function and the width of the device of 4.2 eV and 1.0 μm, respectively.

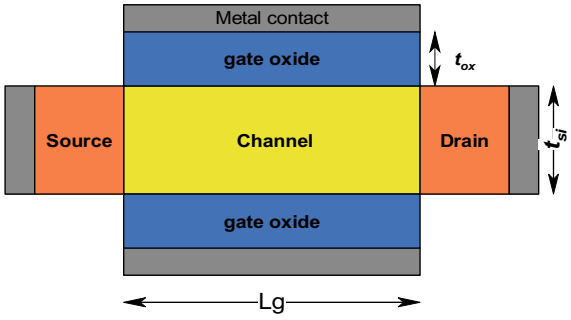

Fig. 1 Structure of DGTFET used for TCAD simulation

3 Results and Discussion

3.1 Analysis of I–V/C-V Characteristics of DGFET

Here in this structure, the intensity of electric field below the gate dielectric is enhanced by applying HfO_2 as a gate dielectric which further results in enhancing the tunneling probability (Tp) of charge carriers as given by Eq. 3, and the same can be visualized from Fig. 2c; where λ is screen length, $\Delta\phi$ is the tunneling barrier potential, E_g is energy band gap of silicon and m* is the electron's effective mass [50].

$$T_p \sim \exp\left[-\frac{4\lambda}{3}.\frac{\sqrt{2m^*}}{h\left(\Delta\phi + E_g\right)}.\left(E_g\right)^{1.5}\right] \tag{3}$$

To understand the electrical characteristics of N type DGTFET, it is important to analyze its energy band diagram for the investigation of charge transport process. Figure 2a depicts the transfer characteristics (I_{ds}–V_{gs}). The insignificant variations in I–V characteristics are noticed for V_{ds} (0.1–0.7 V) at V_{gs} ($0.1 < V_{gs} < 0.3$ V). It is also observed that I_{DS} increases with increasing V_{ds} for higher values of V_{gs}. For V_{gs} = 0.3–0.7 V, a noticeable upward shift in the transfer characteristics is noticed for V_{ds} between 0.1 and 0.3 V and after a further increase in V_{ds} (>0.3 V), Ids shows saturation behavior. Figure 2a depicts that DG TFET possesses very low off current (I_{OFF} ~ 5.0 × 10^{-14} A/μm) which shows the capability to reduce power consumption (~V_{DD} × I_{OFF}) in standby mode for electronic circuits [51]. Simulation results indicate that this structure exhibits a steep subthreshold swing (SS ~ 15 mV/dec), higher on-state current (I_{ON} ~ 0.1 mA/μm), and higher switching current ratio (I_{ON}/I_{OFF} ~ 5 × 10^{10}).

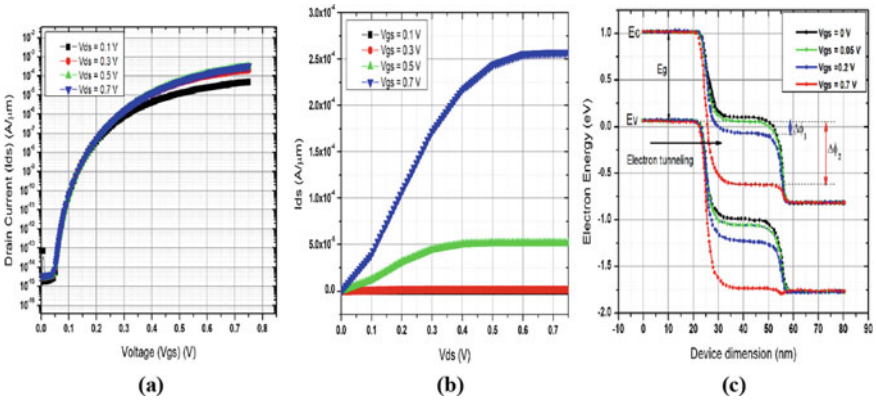

Fig. 2 **a** Transfer characteristics (I_{ds}–V_{gs}) of DG NTFET, **b** Output characteristics (I_{ds}–V_{ds}) of DG NTFET, **c** the energy band diagram of a simulated DG NTFET at V_{ds} of 0.7 V showing tunnel barrier modulation

The current conduction phenomenon can be understood from the TCAD simulations of the energy band diagram as shown in Fig. 2c, which shows the off state (V_{gs} = 0.0 V, $I_{ds} \sim 5 \times 10^{-14}$ A/μm) and the on-state ($V_{gs} = 0.2$ V, $I_{ds} \sim 10^{-7}$ A/μm).

Output characteristics of NDGTFET are shown in Fig. 2b which shows the saturation point for I_{ds} at $V_{ds} > 0.4$ V and for $V_{ds} > 0.7$ V for V_{gs} 0.5 and 0.7 V and higher output impedance can be also predicted for these V_{ds} ranges. In the TFETs, the pinch is shifting to higher values of V_{ds} for higher values of V_{gs} as depicted in Fig. 2b. It is clearly seen that the conduction band of the channel region is not overlapping with the valence band of the source (P+) region ($0.0 \text{ V} < V_{gs} < 0.2$ V) results in a wide tunneling barrier across the source-channel region as shown in Fig. 2c. In this situation, practical device current is very low and at this point, the device current is known as off-current (I_{OFF}). A sharp energy band bending is noticed at the source–channel interface for V_{gs} changes from 0.2 to 0.7 V, which further lowers the tunneling barrier across the source-channel interface, hence increases the Tp so that electrons get transported from the valence band of the source to the conduction band of the channel. The transportation of carriers takes place under the effect of B2BT. For a particular drain voltage, the higher the V_{gs} (higher will be the electric field), the lower will be the tunneling barrier across the source-channel region and higher will be the electron tunneling probability resulting in higher tunneling drain current, Ids (see Eq. 3 and Fig. 2c).

The C–V characteristics for NDGTFET show that the total gate capacitance (C_{gg}) is closely followed by drain capacitance (C_{gd}) for all the values of V_{gs} as shown in Fig. 3 for V_{ds} ranges, 0.1–0.7 V. This can be understood as charges of source-drain regions are directly coupled and governed by B2BT charge transport mechanism in Tunnel FET [23]. Source side tunnel barrier promotes the lower values of C_{gs} (see Figs. 2c and 3) because there are insufficient minority carriers provided by the source, as the source junction is under reverse bias [52–54]. C_{gd} increases for V_{gs} due to reduction in tunneling barrier. Increasing the V_{ds}, a small amount of voltage drop occurs across drain to channel region resulting in lower values of C_{gd} as compared to C_{gs}. Higher the V_{ds}, higher will be the voltage drop across the drain interface results lower values of C_{gd} as clearly shown in Fig. 3. Higher drain voltage results in higher threshold voltage which further reduces energy barrier across the drain side (shifting of the conduction band of drain towards higher energy levels).

Further, the C–V curves are utilized to investigate and analyze the analog behavior of TFET and the same has reported, additionally, the transient simulations are carried out to analyze the impact of V_{DD} and C_L over the miller capacitance (C_{MIL}) in order to investigate the performance of DGTFET inverter.

3.2 Analysis of Analog Performance of DGTFET

As for better amplification action, the FET device should be highly sensitive to the input signal variations and this feature of any amplifier is characterized by a small signal parameter called transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) which determines the

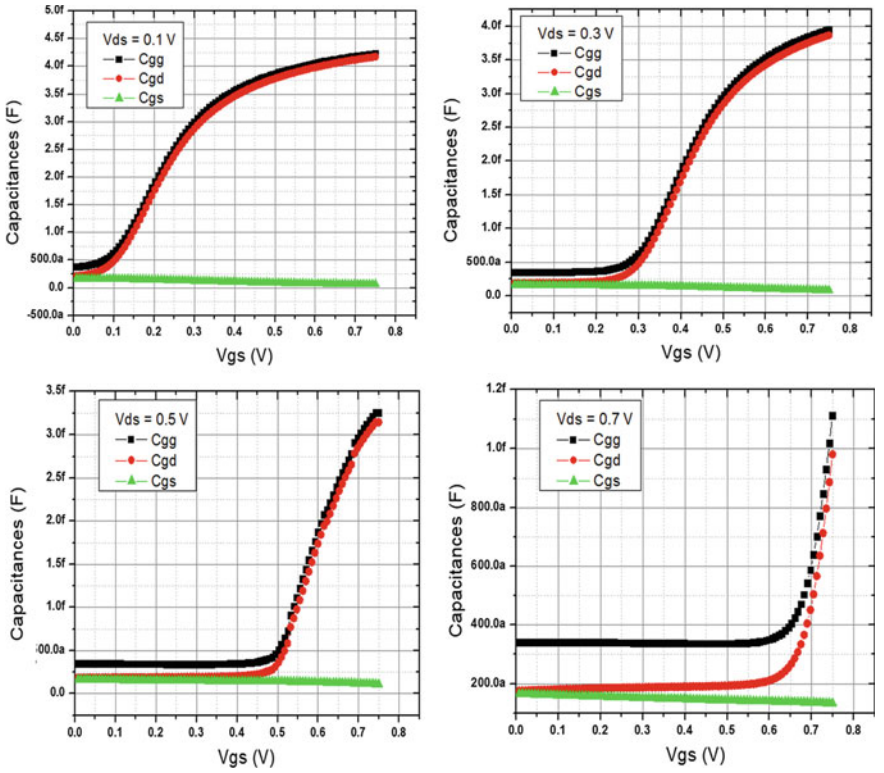

Fig. 3 *C–V* Characteristics of TFET at various drain to source voltage (V_{ds})

gain of the device required for designing of the analog amplifiers. The steep SS of DG TFET leads to higher values of g_m are achieved. Figure 4 shows the g_m for different values of V_{ds} (0.1–0.7 V).

It is also seen from Table 1 that increasing the V_{ds} the ratio ($r = g_{m2}/g_{m1}$) is also increases significantly from 2.33 to 7 for V_{ds} variations (0.1–0.7 V), respectively. From Fig. 4, it is observed that at the lowest value of $V_{ds} = 0.1$ V, the g_m is not showing the sensitive behavior for V_{gs}, i.e., g_m increases only 2.33 times (from 0.75 $\times$ 10^{-4}(s) to 1.75 $\times$ 10^{-4}(s)) for V_{gs} 0.4 V to 0.7 V, respectively, as listed in Table 1. It can be seen from table g_m is more sensitive to V_{gs} for higher values of V_{ds} such that $r = 6$ at $V_{ds} = 0.5$ V and $r = 7$ at $V_{ds} = 0.7$ V, respectively, and this property is suitable for amplification action for FET devices in order to achieve the higher voltage gain.

Another critical parameter for amplification action is short circuit unity gain frequency (f_T) and transit time (t_r) which play a significant role in the analysis of frequency response and carrier transportation time, respectively. High frequency performance of analog circuits is explained in terms of unity gain frequency (f_T) as given by Eq. 4. Figure 5a shows the variation of cut off frequency (f_T) with V_{gs} of

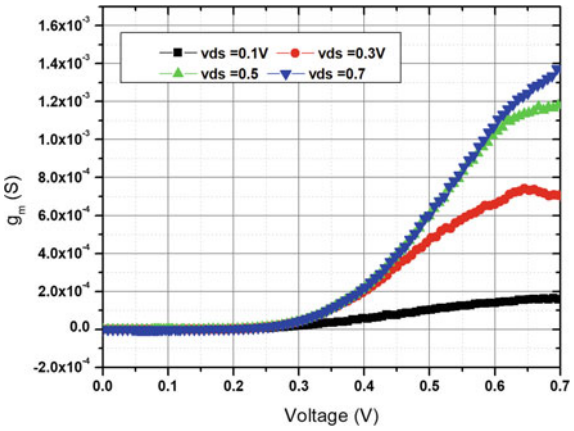

Fig. 4 Impact of V_{ds} voltage on g_m for DGFET performance

Table 1 Listing the Impact of Vds on the g_m

V_{ds} (V)	g_{m1} (S) at $V_{gs} = 0.4$ V)	g_{m2} (S) at (Vgs $= 0.7$ V)	$r = g_{m2}/g_{m1}$
0.1	0.75×10^{-4}	1.75×10^{-4}	2.33
0.3	2×10^{-4}	7×10^{-4}	3.5
0.5	2×10^{-4}	1.2×10^{-3}	6
0.7	2×10^{-4}	1.4×10^{-3}	7

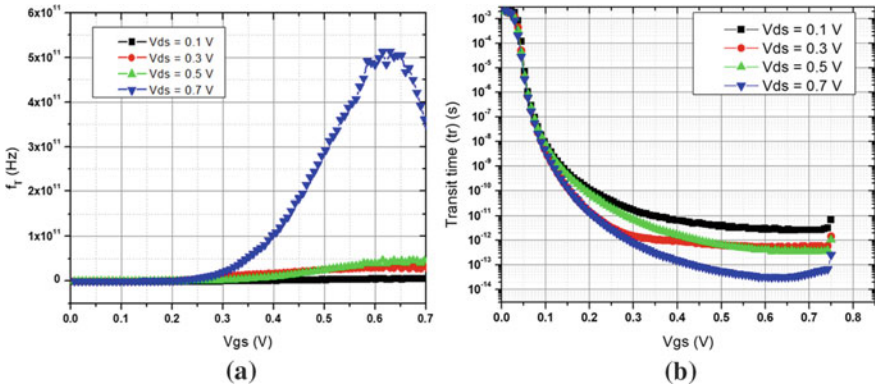

Fig. 5 **a** Impact of drain to source voltage on cut off frequency (f_T) and **b** impact of drain to source voltage transit time (t_r)

DGTFET device for various drain to source voltages.

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4}$$

$$t_r = \frac{1}{20 \cdot \pi \cdot f_T} \tag{5}$$

As given in Eq. 4, the combined effect of different g_m and capacitances (C_{gs}, C_{gd}) can be observed at cut off frequency (f_T). As seen from Fig. 5a, due to the higher gm value, f_T initially increases with increasing V_{GS} and reaches its peak value at 0.1×10^{11} Hz to 5.2×10^{11} Hz for $V_{ds} = 0.1$ V to 0.7 V, respectively. Afterward, C_{gd} for rising V_{gs} increases at a faster pace than gm. For low-power applications, the greater value of f_T makes DG TFET attractive.

The frequency of unit gain (f_T) is also capable of investigating charge transport time in the FET and can be measured in terms of transit time (t_r). The t_r is the time spent in transporting the carriers from the source to drain region and Eq. (5) has provided the same. Figure 5b demonstrates the transit time variance (t_r) with varying gate to source voltage (V_{gs}) for the different drain to source voltage to investigate the effect of drain bias. As the inversion layer is substantially increased as the carriers now travel along a shorter path through the inversion layer and this effect can be clearly depicted from Fig. 5b showing t_r starts reducing with increasing V_{gs}. For a particular value of V_{gs} ($0 < V_{gs} < 0.75$ V), the lower values of transit time (4–0.1 ps) are noticed at the values of $V_{ds} = 0.1$–0.7 V at $V_{gs} = 0.75$ V, respectively, as clearly depicted from Fig. 5b. Higher drain voltage results in a strong electric field in the vicinity of the drain and channel region which efficiently swept out the electrons from channel to drain. The t_r also characterizes the switching ability of the FET devices and for fast switching operations, lower values of the transit time are preferred. Hence, it can be estimated as better switching ability of TFETs at higher drain voltages.

One of the major characteristics of the amplifiers for satisfactory operation is higher bandwidth. GBP is a parameter which shows how much the amplifier is capable to amplify the low frequency message signal and high frequency message signals. Figure 6a, b shows the impact of V_{ds} versus V_{gs} on GBP and TFP parameter, respectively, as given by Eq. 6 and 7.

$$\text{GBP} = \frac{g_m}{20 \cdot C_{gd}}; \tag{6}$$

$$\text{TFP} = \frac{g_m}{\text{Ids}} * f_T \tag{7}$$

It is another crucial investigation of DGFET performance for higher frequency application. From Fig. 6, it is clearly observed that GBP increases initially with Vgs because of increasing behavior of g_m and achieves maximum values of 1.98×10^9 Hz, 1.14×10^{10} Hz, 1×10^{11} Hz, and 2.63×10^{11} Hz for different values of V_{ds}

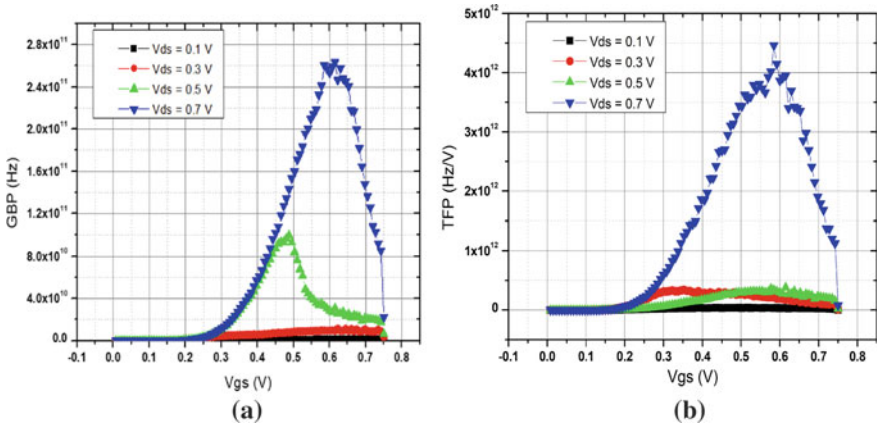

Fig. 6 **a** Impact of V_{ds} on GBP; **b** impact of V_{ds} on TFP

= 0.1 V, 0.3 V, 0.5 V, and 0.7 V, respectively. TFP is also following the same trend such that it saturates at its maximum value of 4.31 × 10^{10} Hz/V, 3.42 × 10^{11} Hz/V, 3.81 × 10^{11} Hz/V, and 4.46 × 10^{12} Hz/V for different values of V_{ds} for 0.1 V–0.7 V, respectively (see Fig. 6b). The driving point behind the GBP variations is the combined effect of g_m and C_{gd}, i.e., for a particular range of V_{gs}, g_m is dominated by C_{gd} and afterward C_{gd} starts dominating over g_m (see Figs. 2 and 4) resulting in peak values in GBP. It is observed that as V_{ds} increases, the peaks of the GBP curves start shifting toward the higher values of V_{gs}; GBP peak at V_{gs} = 0.49 V for V_{ds} = 0.5 V and GBP peak V_{gs} = 0.6 V for V_{ds} = 0.7 V as depicted from Fig. 6a. TFP for V_{ds} = 0.7 V starts falling for V_{gs} > 0.6 V due to falling in f_T (see Fig. 5a).

3.3 Transient Performance of TFET to Analyze the Impact on Miller Capacitance (C_{MIL})

In this section, the impact of supply voltage (V_{DD}) and load capacitance (C_L) on the Miller capacitance (C_{MIL}) which is formed by B2BT tunneling has been investigated. Several parameters for digital applications are computed and listed for inverter based on DG TFET. To carry out the transient analysis, a 4 ns time period digital pulse (V_{in}) is applied at the input of DG TFET inverter and output digital waveform is measured at node V_{out}. Figure 7 has shown the Vout for various C_L in order to evaluate the inverter performance in terms of rise time (T_r), fall time (T_f), delay (t), peak overshoot (V_p), % peak overshoot, miller capacitance (C_{MIL}). It is clearly seen from Table 2 and Fig. 7 that the % peak overshoots are diminishing from 42.8 to 2.14% and total delay increasing (0.18–1.9 ns) with increasing the C_L (10–200 fF). This behavior can be explained by taking the impact of miller capacitance as given by Eqs (8 and 9). The extent of the voltage peak overshoot can be estimated from the

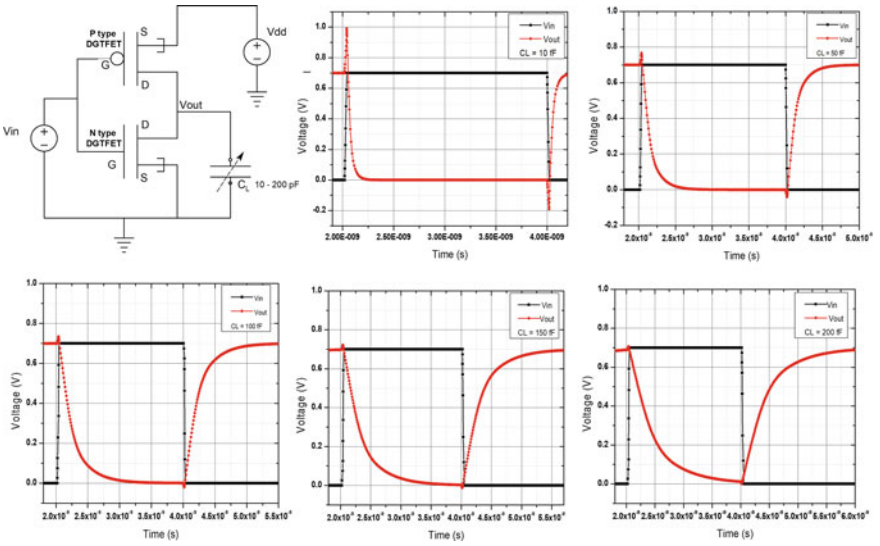

Fig. 7 Input and output waveforms of double gate TFET inverter for various capacitive load (C_L)

Table 2 Impact of load capacitance (C_L) on the transient performance of DGTFET

V_{DD} 0.7 V	C_L (fF)	Rise time T_r (ns)	Fall time T_f (ns)	Delay (ns)	V_p (V)	(%V_p)	C_{MIL} (fF)
1	10	0.2	0.16	0.18	0.30	42.80	11.27
2	50	0.60	0.55	0.575	0.08	11.42	6.45
3	100	1.2	1.0	1.1	0.04	5.71	6.06
4	150	1.4	1.5	1.45	0.025	3.57	5.55
5	200	2	1.8	1.9	0.015	2.14	4.32

following equations based on the law of charge conservation (Eqs. 6 and 7) [55, 56].

$$C_{MIL} \cdot (V_M - V_{DD}) + C_L \cdot V_M = V_{DD} \cdot (C_{MIL} + C_L) \tag{8}$$

$$V_p = V_M - V_{DD} = C_{MIL} \cdot V_{DD}/(C_{MIL} + C_L) \tag{9}$$

where C_{MIL} denotes the Miller capacitance across drain and gate nodes consisting of both comprising inverter structure with N DGTFET and P DGTFET, C_L represents the load capacitance connected externally, maximum output voltage (V_{out}) represented by V_M, Vp is the output peak overshoot voltage, and V_{DD} is the supply voltage. In silicon-based TFETs, these equations clearly demonstrate the effect of C_{MIL} on V_p. Increasing load capacitance (C_L) raises the time constant (R_C), and thus increases the drain node's charge and discharge time in accordance with Eq. 10. This

effect can be validated in Fig. 7 and the parameters are shown in Table 2, showing that the delay increases with the C_L.

$$V = V_o\left(1 - e^{-t/RC_L}\right) \tag{10}$$

At the same instant, it is also observed that voltage peak overshoot occurs in the transient performance of the TFET inverter for each capacitance load. Figure 7 shows the diminishing voltage peak overshoots with an increasing load capacitance. The % peak overshoots are directly proportional to C_{MIL}. Table 2 has listed the values of C_{MIL} for various C_L. The charge conservation equations (Eqs. 8 and 9) are applied to compute the value of C_{MIL} (listed in Table 2) and it is found that the miller capacitance (C_{MIL}) decreases (11.27–4.32 fF) with increasing C_L (10–200 fF), hence results in diminishing % peak overshoots. From the detailed discussion, it can be understood that to diminish the % peak overshoots, the higher values of load capacitance need to be considered so that impact of C_{MIL} gets diminished in FTETs.

Figure 8 shows the impact of V_{DD} on the Miller Capacitance (C_{MIL}). The transient performance of DGTFET inverter is listed in Table 3 has listed its performance parameters. Upon increasing the V_{DD}, the delay of the inverter decreases, and shows saturation in delay for V_{DD} from 0.6 to 0.8 V. Increasing V_{DD} results in higher drain current, but for higher drain voltages, the drain current gets saturated as shown in Fig. 2a. From Table 3, it is clearly seen that the delay has decreased by 50% (from 0.8 to 0.4 ns) for V_{DD} from 0.5 to 0.6 V, 37.5% (from 0.4 to 0.25 ns) for V_{DD} from 0.6 to 0.7 V, and by 20% (0.25–0.2 ns) for V_{DD} from 0.7 to 0.8 V, respectively. It is also observed that a 50% decrease in delay for the V_{DD} from 0.5 to 0.6 V and only

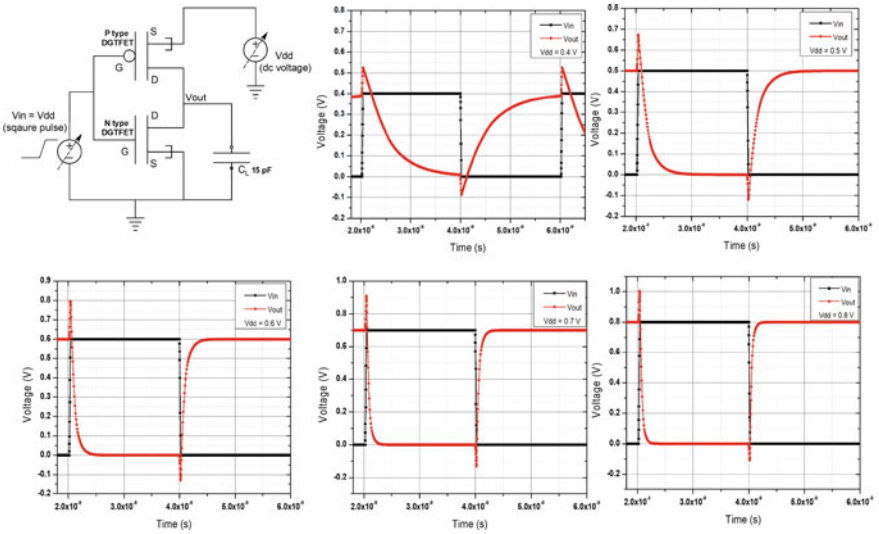

Fig. 8 Input and output waveforms of double gate TFET inverter at various drain to source voltage (V_{ds})

Table 3 Impact of V_{DD} on the transient performance of DGTFET

C_L = 15 fF	V_{DD} (V_{DD} = V_{in})	Rise time T_r (ns)	Fall time T_f (ns)	Delay (ns)	V_p (V)	(%V_p)	C_{MIL} (fF)
1	0.5	0.8	0.8	0.8	0.175	35	8
2	0.6	0.4	0.4	0.4	0.2	33	7.5
3	0.7	0.25	0.25	0.25	0.22	31.4	6.88
4	0.8	0.2	0.2	0.2	0.21	26.25	5.35

20% decrease in delay for V_{DD} from 0.7 to 0.8 V due to saturation of drain current at higher drain voltages.

An opposite trend is observed for the % peak overshoot; % V_p does not show significant variation for V_{DD} from 0.5 to 0.6 V, it only changes from 35 to 33%. However, for the V_{DD} range from 0.7 to 0.8 V, there is a significant variation in % V_p are noticed during the simulations from 31.4 to 26.25%. Simulations results also investigated that miller capacitance (C_{MIL}) continuously decreasing from 8 to 5.35 fF for increasing the V_{DD} from 0.5 to 0.8 V and this impact is also noticed in the % peak voltage overshoots from 35 to 26.25% which further results in better delay performance of TFET inverter (see Fig. 8 and Table 3).

4 Conclusion

Simulations results investigate that the quantum band to band tunneling (B2BT) charge transport process is responsible for current conduction in DGTFETs producing steep subthreshold swing (SS ~ 15 mV/dec) and high I_{ON}/I_{OFF} ratio ~10^{11} with the presence of very low leakage current (~5 × 10^{-14} A/μm), and thus can be considered for low-power applications. Implementation of *I–V*/*C–V* data sets in the form look table coded with verilog-A model can be considered as one of the effective way to analyze circuit behavior of DGTFETs device structure. Simulation results for GBP, TFP, transit time (t_r), g_m, f_T investigate that the DGTFET device structure can be considered for analog applications. Findings from transient analysis describe the existence of miller capacitance (C_{MIL}) present at gate-drain node of TFET inverter, which is affected by voltage (V_{DD}) and load capacitance (C_L). The combined study of analog and transient parameters of TFET device structure describes the suitability of TFET for integrated circuits applications.

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