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Rigorous Study of Double Gate Tunneling Field Effect Transistor Structure Based on Silicon

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ABSTRACT

Increased static and dynamic power dissipation in the integrated circuits (ICs) are the main obstacle for growing demands of smart phones and laptops, which require semiconductor devices having low power operation. As the conventional MOSFET has a thermodynamic limit of 60 mV/decade at 300 K on subthreshold slope (SS), so the device based on the mechanism other than diffusion over a thermal barrier came into existence. In this regard, Tunnel-FET (TFET) has emerged as a promising replacement. Due to its lower subthreshold slope (<60 mV/decade at 300 K), reduced OFF-current (I_{OFF}), reduced power consumption, and negligible short channel effects, TFETs have achieved a lot of attention in the recent years. In the present research work, double-gate TFET (DG-TFET) device has been investigated. The simulation result shows a very good I_{ON}/I_{OFF} ratio (10^{12}) and low SS (~41.54 mV/dec). The DG-TFET has very low off current, I_{OFF} (~10^{-17} A/μm) and ON-current of (I_{ON}) ~10^{-5} (A/μm) using gate bias in the vicinity of 0.5. In addition, we have optimized the device parameters, thus improving the I_{ON} current and the I_{ON}/I_{OFF} ratio yield for two kinds of technologies (using HfO_2 or SiO_2 as gate dielectric). A comparison between the two technologies was made. Gate to drain (C_{gd}) capacitance as function of gate to source voltage V_{GS} as well as drain to source voltage V_{DS} at frequency $f = 1$ MHz, C_{gd} is weaker using SiO_2 as gate dielectric compared to HfO_2.

KEYWORDS: Tunnel FET, High-κ Dielectric, Subthreshold Slope (SS), Band-to-Band Tunneling (BTBT), Quantum Mechanical Transport QMT.

1. INTRODUCTION

The inability, to reduce power density with each progressive technology node has been a dominant constraint for modern semiconductor players. Various techniques have been proposed to reduce computational power spanning from the architecture level to the fundamental semiconductor device level are being actively explored. Tunnel Field-effect transistors (TFETs), based on band-to-band tunneling (BTBT), a quantum mechanical transport (QMT) phenomenon has gained a lot of attention in the modern research community due to its potential for reducing power dissipation for advanced integrated circuits (ICs). This ever increasing interest owes to their feasibility to overcome the 60 mV/dec subthreshold slope limitation of the standard MOSFETs,[1–4] as well as compatibility.[5] TFET is basically a *p–i–n* structured device. The device operation requires reverse bias to realize tunneling phenomenon between sources and drain regions with a sufficient level of gate voltage.[6–12]

Recently, many research groups across the world have reported many proposed devices designed to overcome the on-state current limitation in TFET. The double gate TFET (DG-TFET) with high-κ dielectric is an effective way to improve the on-current (I_{ON}), while taking advantage of steeper subthreshold slope and lower OFF-current.[12–23]

2. ANALYTIC ANALYSIS OF SENSITIVITY

For MOSFETs, the analytic expression for current in a subthreshold regime, where most of current modulation as a function of gate voltage occurs, is given approximately by:[12]

$$I_{DS} = I_{OFF} \exp\left(\frac{V_G}{V_{th}(1+(C_S/C_{OX}))}\right) \quad (1)$$

where V_{th} equals kT/q and I_{OFF} is the OFF current at $V_G = 0$. C_S represents the semiconductor capacitance and it is a function of ε_{ch} and t_{ch} for short-channel devices.

In case of TFETs, the approximate equation for the I–V characteristics leads as follows:[12]

$$I_{DS} = I_{OFF} \exp\left(A\sqrt{m^*}\left(\sqrt{E_g + qV_G} - \sqrt{E_g}\right)\right) \quad (2)$$

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where A is the total tunneling distance which is the sum of natural scaling length λ and source depletion width W_D ($A = \lambda + W_D$), q is the unit charge and E_g and m^* are bandgap and effective mass of the channel material, respectively.

The subthreshold swing of a device is defined as: the change in gate voltage which must be applied in order to create a one decade increase in the output current[6, 12]

$$S = \frac{dV_{GS}}{d(\log I_{DS})}(\text{mV/dec}) \quad (3)$$

That the tunneling probability, $T(E)$ is given by:[12]

$$T(E) \propto \left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3\lfloor e \rfloor \bar{h}(E_g + \Delta\Phi)} \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} t_{si}} \right) \Delta\Phi \quad (4)$$

In Eq. (4), m^* is the electron effective mass, E_g is band gap, $\Delta\Phi$ is the energy range over which tunneling can take place, and t_{ox}, t_{si}, ε_{ox}, ε_{si} are the oxide and silicon films thickness and dielectric constants respectively, and $\bar{h}$ is the reduced Planck's constant. The tunneling window ($\Delta\Phi$) in the tunneling probability is written as follows:[12]

$$\Delta\Phi = E_V^{ch} - E_C^S$$

3. STRUCTURE AND SIMULATION METHODOLOGY

The electrical performance of DG-TFET was investigated using Silvaco TCAD Atlas 2D software V5.15.32 R.[10]

The double gate provides electrostatic control over the channel in which the drain field line cannot affect or disturb the source-to-channel barrier and it promisingly reduces the short channel effects. The DG-TFET, adopted in the present research work is shown in Figure 1, having three regions: n-type semiconductor bar forming source and channel region, and p-type semiconductor by forming drain region. In between two regions an intrinsic semiconductor layer is sandwich. The quantum mechanical transistor (QMT) has reached such small dimensions for doping concentration gradients are: 7.5×10^{20} cm^{-3}, 10^{10} cm^{-3} and 5×10^{18} cm^{-3} for the source, intrinsic, and drain regions respectively. Doping has been optimized to create the maximum ON-current (I_{ON}), while keeping OFF-current (I_{OFF}) low. In order to have a minimal I_{OFF}, the doping of the source is slightly lower compared to that of the drain.

The flow chart for present research work is shown in Figure 2.

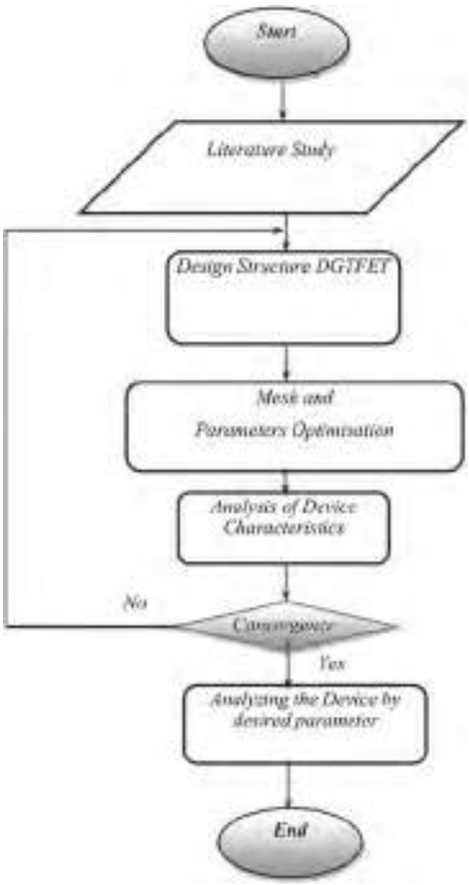

Fig. 2. Atlas resolution algorithm of double gate TFET.

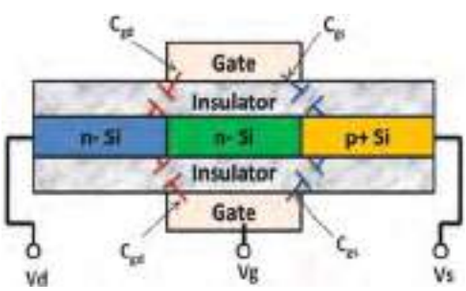

Fig. 1. Structure of double gate TFET (DG-TFET).

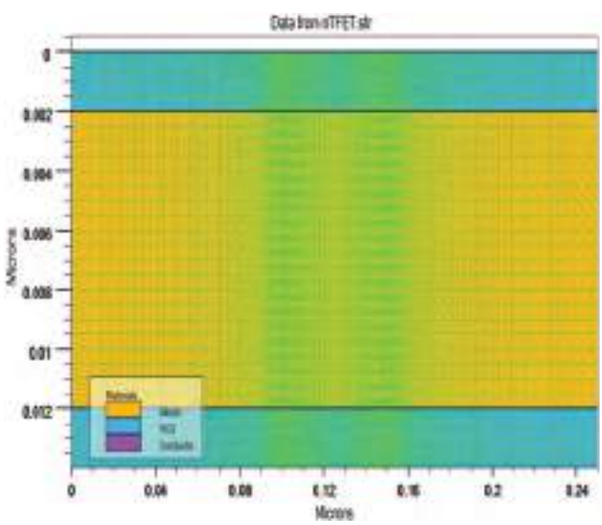

Fig. 3. Tony plot display using 2D mesh of double gate TFET.

Table I. Design parameters considered for simulation.

Parameters	Values
Gate length (L_g)	50 nm
Drain and source lengths (L_D, L_S)	100 nm
Oxide thicknees (t_{ox})	2 nm
Channel thicknees (t_{si})	10 nm
Source concentration (N_a)	7.5×10^{20} cm^{-3}
Intrinsic concentration (N_d)	10^{10} cm^{-3}
Drain concentration (N_d)	5×10^{18} cm^{-3}
Gate voltage (V_g)	1.0 V
Supply voltage (V_{dd})	0.5 V

Table II. Parameters oxide gate used in simulation.

	Oxide gate			
Parameters	SiO_2	Si_3N_4	ZrO_2	HfO_2
Bandgap (eV)	9	5.3	5.7–5.8	4.5–6
Relative dielectrics constant	3.9	7.9	22	25

The DG-TFET, as shown in Figure 1, consists of $p+$ source, intrinsic channel and $n+$ drain. The local tunneling models were used to calculate tunneling current from the source to drain with varying gate voltage (V_{GS}).

The I–V characteristics of DG-TFET have been plotted and investigated by using Newton method to solve numerical system. The choice of the mesh under atlas is a vital step to have a convergence. Figure 3 shows the tony plot display using 2D mesh of DG-TFET.

The gate dielectric layer must be sufficiently thin and therefore, we have taken the oxide thickness t_{ox} of 2 nm. The work function of the metal work function, Φ_M used is 5.2 eV. The drain, source and intrinsic region lengths, L_D, L_S and L_G are taken as: 100 nm, 100 nm and 50 nm respectively. The silicon thickness t_{Si} is 10 nm for DG-TFET. All the physical parameters use in work is tabulated in Table I. The electrical parameters of used dielectric materials is shown in Table II.[19–21]

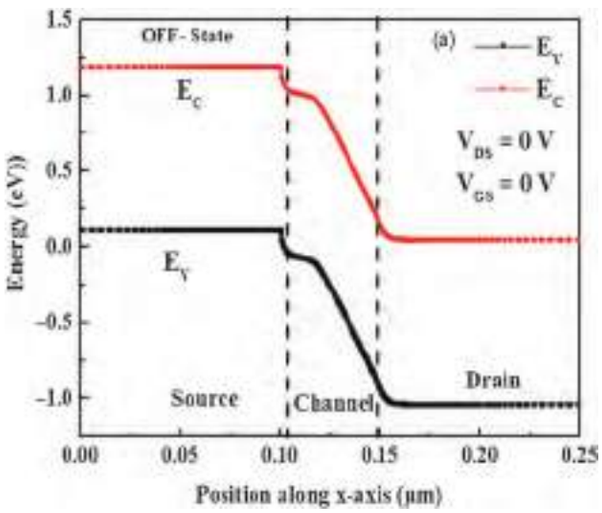

Fig. 4. Energy band-diagram (a) at $V_{GS} = 0.0$ V (OFF-state) for DG-TFET.

4. RESULTS AND DISCUSSION

Using 2-D numerical device simulator, the electrostatic performance of DG-TFET is analyzed. Figures 4 and 5 show the simulated energy band diagram of DG-TFET, shown in Figure 1. With the help of the energy band diagram the ON–OFF state conduction phenomenon of the DG-TFET is explained. As shown in Figures 4 and 5, when $V_{GS} = 0.0$ V and $V_{DS} = 0.0$ V. The device is in OFF-state with very large tunnel barrier width, and therefore the electrons do not have enough energy to move from the valance band of the source to the conduction band of the channel. On application of sufficiently high gate voltage

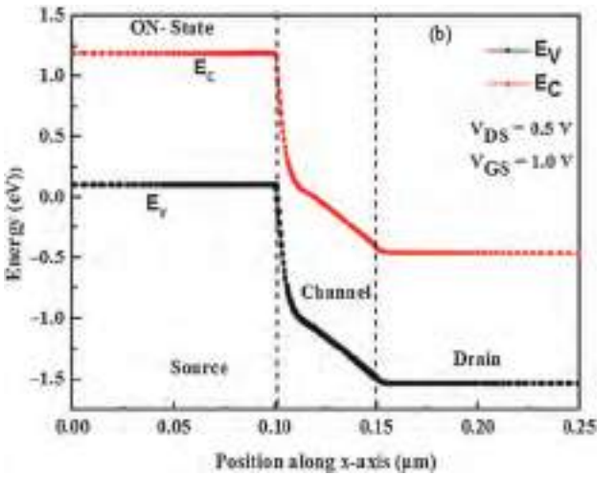

Fig. 5. Energy band-diagram at $V_{GS} > 0.0$ V (ON-state) for DG-TFET.

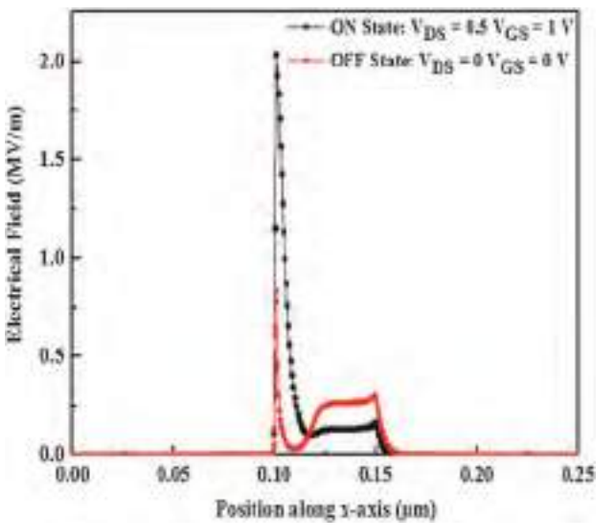

Fig. 6. The electric field behavior analysis of DG-TFET.

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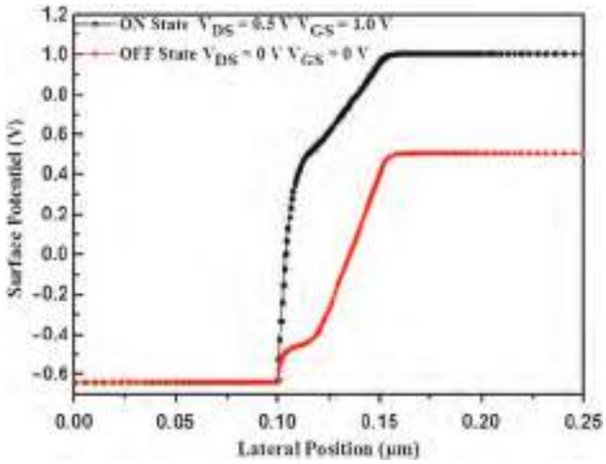

Fig. 7. Potential surface for DG-TFET structure for $V_{GS} = 0.0$ V and $V_{GS} = 1.0$ V.

(i.e., $V_{GS} = 0.5$ V and $V_{DS} = 1.0$ V), the width of tunneling barrier is reduced and the device switches to ON-state.

When the device switched from the OFF-state to the ON-state, an increase in the electric field is observed. It has been observed that, the tunnel width decreases and there is a shift of the conduction band downwards. Thus, the gradual enhancement of the gate bias degrades the barrier width and causes an increased tunneling of carriers, indicated in Figure 5. Figures 6 and 7 shows the internal electric filed and surface potential inside the device. In both (Figs. 6 and 7), there is relative comparison between ON and OFF-state.

Since, HfO_2 is the core material in the gate stack in high-κ metal gate devices for technology nodes less than 45 nm,[22,23] therefore we have used it in our device simulations. Figure 8 shows the transfer characteristic of DG-TFET. As shown in Figures 9((a) linear (b)) semilog plot), the variation of leakage current (I_{OFF}) is almost constant for all values of V_{DS}.

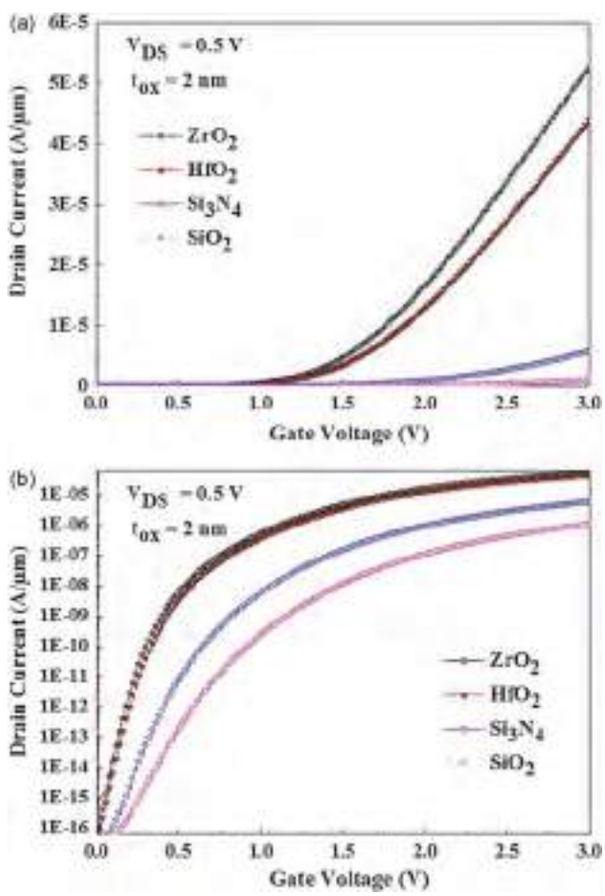

Fig. 8. Plot of the transfer characteristic (I_{DS}–V_{GS}), regarding different gate oxide in Atlas of a DG-TFET device with $L_G = 50$ nm (a) linear (b) plot Semilog plot.

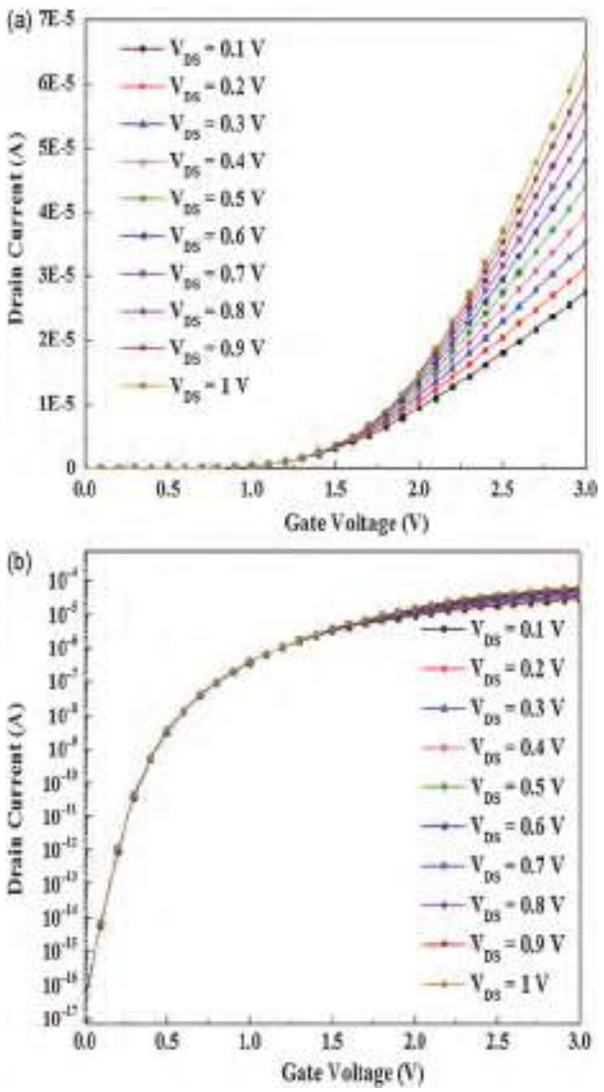

Fig. 9. Device transfer characteristics for double gate N-TFET with a variation of V_{DS} (a) plot linear (b) plot Semilog.

Table III. Lists of the computed electrical parameters of the DG-TFET.

Parameters	Oxide gate			
	ZrO_2	HfO_2	Si_3N_4	SiO_2
V_{th} (V)	0.2	0.2	0.45	0.5
SS (mV/decade)	41.59	41.54	43.99	46.89
I_{ON} (A/μm)	5.26×10^{-5}	4.38×10^{-5}	5.84×10^{-6}	1.118×10^{-6}
I_{OFF} (A/μm)	5.02×10^{-17}	4.03×10^{-17}	2.52×10^{-17}	2.43×10^{-17}
I_{ON}/I_{OFF}	$1{,}05 \times 10^{+12}$	$1{,}09 \times 10^{+12}$	$2{,}318 \times 10^{+11}$	$4{,}61 \times 10^{+10}$

It is evident from the results that, the drain current performance is improving with replacement of high-κ gate materials instead of using conventional SiO_2. Threshold voltage (V_{th}) of DG-TFET reduces with high-κ gate, as shown in Table III due to improved electrostatic filed inside tunneling region. This is also a scientific indication for lower power supply.

The output characteristic is improved with increasing drain voltage and achieves its optimum value for drain voltage V_{DS} equal to 1.0 V. The use of high–high-κ improves the output characteristics for a low gate voltage of the order of 0.5 V. An increase in the drain voltage V_{DS} greatly increased I_{ON} current but had no effect on the threshold voltage.

The various capacitance parameters such as gate-to-drain (C_{gd}), gate-to-source (C_{gs}) and drain-to-source (C_{ds}) have been extracted from AC analysis of the designed structure. Figures 10 and 11 show the CV analysis results for DG-TFET. CV analysis of DG-TFET is done at 1 MHz frequency. It is observed that C_{gd} increases with increasing gate voltage, this is due to the reduction of the potential barrier (as we saw in the energy band diagram, shown in Fig. 7).

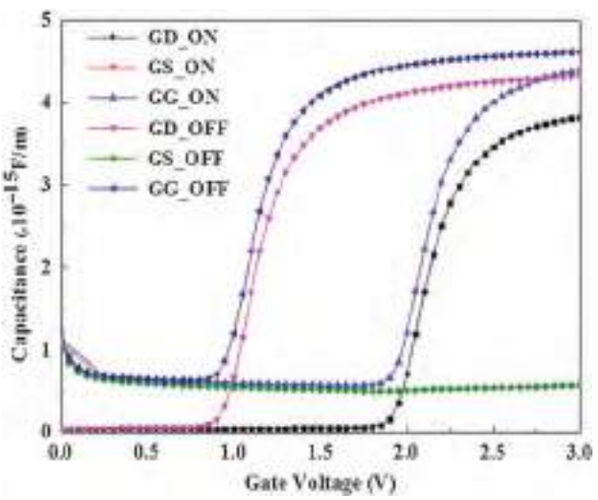

Fig. 10. Capacitance voltage characteristics showing the gate (C_{gg}), gate to source (C_{gs}), and gate to drain (C_{gd}) capacitance as function of gate to source V_{GS} for for DG-TFET extracted at $f = 1$ MHz.

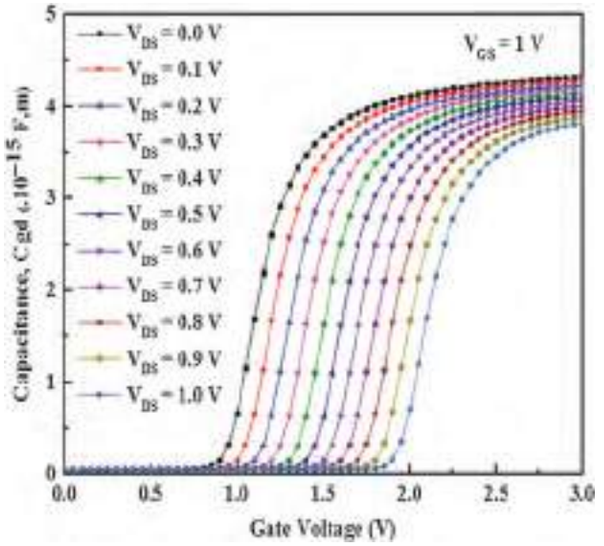

Fig. 11. Gate-to-drain capacitance C_{gd} as a function of gate to source voltage V_{GS} for different drain to source voltage V_{DS} for DGTFET extracted at $f = 1$ MHz.

Figure 10 shows comparison between available capacitance such as: (C_{gd}), gate-to-source (C_{gs}) and drain-to-source (C_{ds}). The capacitance voltage (CV) characteristics showing the gate (C_{gg}), gate to source (C_{gs}), and gate to drain (C_{gd}) capacitance as function of gate to source V_{GS} for for DG-TFET. Due to the presence of a source side tunnel barrier, the gate-to source capacitance (C_{gs}) is very small. It explains that BTBT has negligible influence in the charge distribution of a DGTFET. While, C_{gd} (gate-to-drain capacitance) reflects the entire gate capacitance (C_{gg}). The C_{gd} decreases and shifts to the right when, the drain voltage (V_{DS}) increases. This is due to the reduction of the tunnel distance as was observed on the energy bands, this observation was ensured by the simulation.

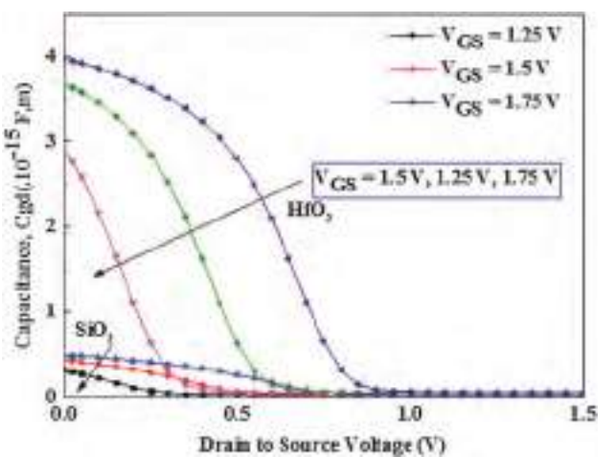

Fig. 12. Gate-to-drain capacitance C_{gd} as a function of drain to source voltage V_{DS} for different gate to source voltage V_{GS} for DG-TFET extracted at $f = 1$ MHz (SiO_2 and HfO_2).

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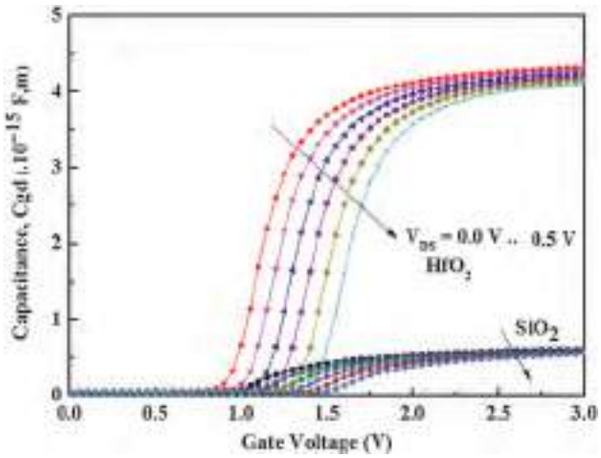

Fig. 13. Comparison between gate-to-drain capacitance C_{gd} as a function of drain to source voltage V_{GS} (SiO_2 and high-κ) for DG-TFET extracted at $f = 1$ MHz.

Figures 12 and 13 show CV characteristics of DG-TFET for SiO_2 and HfO_2 (as oxide gate).

In ON-state, changing Oxide Gate gives a smaller C_{gd}, inv when we use SIO_2 as oxide gate than high-κ '(HfO_2). C_{gd} is significantly reduced in the inversion region (a difference of 3 decades) despite there is not a big difference in the current (Fig. 8). In order to improve switching speed of DGTFET, we have to use the both oxide gate (HfO_2 and SiO_2). The results are compared with those plotted in literature A good agreement is observed between both work.[23]

5. CONCLUSION

In this paper, we designed and analyzed the *n* type double gate tunnel Field Effect Transistor (DG-TFET), to address the requirements for ULP (Ultra-Low-Power) applications. The performance of the DG-TFET design in terms of power, the DG-TFET supports voltage scaling and works for supply voltage from 0.1 to 1.0 V. In this paper a double gate TFET (DG-TFET) electrical characteristics is investigated using the 2-D simulation with of standard scientific computing tool, Silvaco. The device electrical parameters such as drain current, and threshold voltage, subthreshold slope (SS), leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio have been obtained Threshold voltage of DG-TFET reduces due to improved electrostatic filed inside tunneling region. This is also a scientific indication for lower power supply.

It is evident from, the results that drain current is improving. Current, I_{ON} it value very low close to 10^{-5} and I_{OFF} close to 10^{-17} for the SiO_2 gate oxide and high-κ (HfO_2). The ratio I_{on}/I_{OFF} is very large, whatever the nature of the gate oxide, so SS is weak. Whatever the nature of the chosen oxide, this device gives excellent I_{ON}/I_{OFF} ratio of 10^{12} for a very.

They have been consistent with other studies having noble information. The results for SiO_2 oxide have been improved. The CV characteristics of DG-TFET are also investigated.

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