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High-k Double Gate Junctionless Tunnel FET with Tunable Bandgap

Shiromani Balmukund Rahi,[*a] **and Bahniman Ghosh,**[b‡]

In the present work, the performance of a hetrostructure double gate junctionless tunnel FET (HJL-DGTFET) having tunable source-bandgap has been analyzed using 2D simulation technique. The tunable source HJL-DGTFET shows high ON-current $\approx 6.5\times10^{-5}$ A/μm and very low OFF-current $\approx 4.8\times10^{-17}A/\mu$m. The device shows point subthreshold slope $\approx$ 36.2 to 26.8 mV/decade and the average subthreshold slope $\approx$ 86.1 to 84.2 mV/decade for 0.0% to 40.0% Ge-mole fraction at room temperature with I_{ON}/I_{OFF} ratio of 10^{12}. The excellent switching characteristics and steeper subthreshold slope at room temperature indicates that this is promising candidate for replacement of bulk MOSFETs. In this article, optimization of device parameters such as the oxide thickness (t_{ox}), gate dielectric and spacer has also been discussed in details.

1 Introduction

In recent years, green transistor has attracted a lot of attention as a replacement of aggressively scaled conventional bulk MOSFETs for low power applications. The rapid down-scaling of conventional bulk MOSFETs below 45nm introduced undesirable effects such as gate leakage current, short channel effects (SCEs) and hot carriers effects (HCEs), which led to extreme degradation in device performance [1]. One of the fundamental limit of conventional MOSFETs is subthreshold slope (SS) at room temperature with a minimum value of 60mV/decade which can be obtained from [1,2]:

$$SS = \frac{dV_g}{d\psi_s}\frac{d\psi_s}{d(log_{10}I_d)} \approx (1+\frac{C_d}{C_{ox}})log_{10}\frac{K_BT}{q} = 2.3\frac{K_BT}{q}\ , \quad (1)$$

where ψ_s is the surface potential, V_g is the gate voltage, C_{OX} is the oxide capacitance, C_d is the depletion capacitance and k_BT/q is the thermal voltage (26mV/dec at 300K).

In down-scaling approach, conventional Si MOSFETs are approaching towards the end of technology roadmap. To overcome this limitation, various alternate devices are being proposed such as multigate MOSFET (FinFET and gate all around FETs) and ultra-thin body (UTB) devices. These proposed devices could be less attractive in ultra scaled regime to fulfill the need of low power applications such as computer and mobile technology [3–6]. For low power applications, subthreshold slope (see Eq. (1)) plays very significant role [1]. The electrical characteristics of TFETs is less influenced by short channel effects (SCEs) [7–11] and also breaks the physical limitations of bulk MOSFET due to $SS < 60mV/dec$ at room temperature. The lower subthreshold slope value for TFETs allows power supply (V_{DD}) scaling. The scaling of supply voltage, improves the leakage power reduction $(P = I_{OFF} \times V_{DD})$ for TFETs devices in comparison to bulk MOSFETs [2].

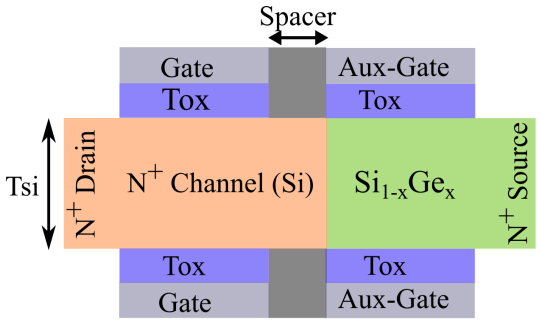

Fig. 1 Schematic view of hetrostructure doublegate junctionless Tunnel FET (HJL-DGTFET).

The hetrostructure double gate junctionless tunnel FET (HJL-DGTFET) is an improved version of conventional TFET. The HJL-DGTFET does not have P-N junction at source/channel and channel/drain interface, as a result has lower value of leakage current than conventional TFETs [12–15]. The silicon based TFETs have large bandgap and as a result have low band-to-band (B2B) tunneling and lower drive current (I_{ON}). To improve the drive current of TEFTs, silicon germanium $(Si_{1-x}Ge_x)$ alloys and III-V semiconductor based low bandgap TFETs have been demonstrated [16,17].

In this paper, HJL-DGTFET with improved device performance is suggested for low power applications. In this device, the impact of germanium mole fraction, oxide thickness, gate spacer and gate oxide material on the device performance has been studied and discussed in detailed.

2 Adoption of tunable band behavior in JL-TFET

The TFET devices comparatively have small leakage current and low subthreshold slope against the bulk MOSFETs but suffer from low on-current (I_{ON}). To improve the

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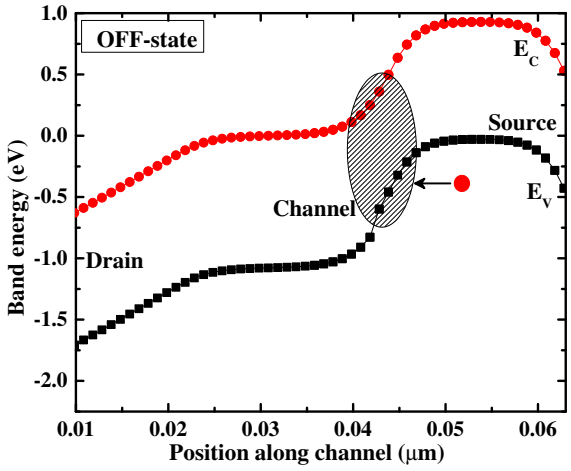
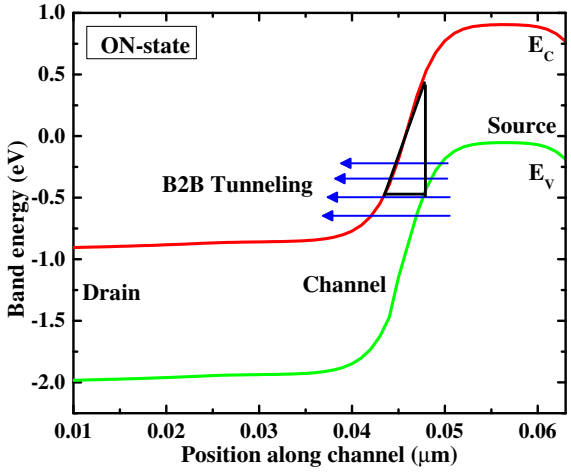


(a)



(b)

Fig. 2 (a) Energy band-diagram at V_{GS} = 0.0V and (b) Energy band-diagram at $V_{GS} > 0.0$V for HJL-DGTFET.

I_{ON} of TFETs, various approaches such as heterostructure source/channel, low band gap semiconductor, high-k gate materials and inclusion of strain effect has been adopted. The bandgap of HJL-DGTFET at the source/channel interface is transformed into a tunable form by using the band engineering via the epitaxially grown $(Si_{1-x}Ge_x)$ layer on silicon. The epitaxially grown $(Si_{1-x}Ge_x)$ layer on silicon creates lattice mismatch between Si/$(Si_{1-x}Ge_x)$ as a result strain originates at the interface. The lattice constant of $Si_{1-x}Ge_x$ with mole fraction of germanium could be calculated by Vegard′s rule [18] as follows:

$$a_{SiGe} = a_{Si} + x(a_{Ge} - a_{Si}) \,, \tag{2}$$

where a_{si} is the lattice constant for silicon, a_{Ge} is the lattice constant for germanium, x is the mole fraction of Ge in $Si_{1-x}Ge_x$ and a_{SiGe} is the lattice constant for $Si_{1-x}Ge_x$. The induced strain at the Si/$(Si_{1-x}Ge_x)$ interface due to lattice mismatch reduces the effective bandgap between conduction band of channel and valence band of source in the tunneling region. The effective Ge-mole fraction dependent bandgap of tunneling region in HJL-DGTFET is calculated from [19–23]:

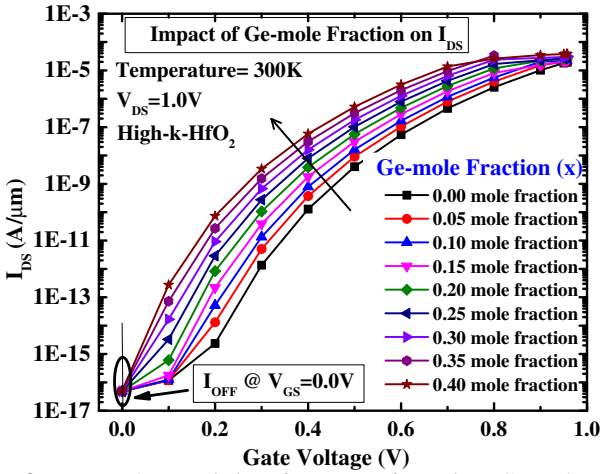


Fig. 3 Turn-on characteristics of JL-TFET for various Ge-mole fractions in $Si_{1-x}Ge_x$ source. The device is biased by control gate, auxiliary gate and drain-source voltage at V_{GS} = 0.0V to 1.0V, V_{G-Aux} = 0.0V and V_{DS} = 1.0V respectively.

$$E_g^{SiGe} = 1.084 + 0.42x \,, \tag{3}$$

where E_g^{SiGe} is the bandgap for the $(Si_{1-x}Ge_x)$.

3 Band-to-band-tunneling current modeling approach

The schematic of the HJL-DGTFET device used in the study is shown in Fig.1. In the HJL-DGTFET, current conduction strongly depends on the tunneling width (λ) and is controlled by the gate voltage. The band diagram of the device for off-state and on-state is shown in Fig. 2(a) and Fig.2(b) respectively. The tunneling of charge carriers in the device strongly depends on the bandgap (E_g) (see Fig.2). The epitaxially grown $(Si_{1-x}Ge_x)$ alloy on silicon causes the compressive strain on both Si and $(Si_{1-x}Ge_x)$. Induced strain in alloy modifies the band-structure as well as band gap of $Si_{1-x}Ge_x$ which can be calculated by Eq. (3) with Ge-mole fraction. In the tunneling region of HJL-DGTFET, at the heterostructure source/channel interface $Si_{1-x}Ge_x$ have smaller bandgap than silicon as a result tunneling probability will be increased. The tunneling probability for the HJL-DGTFET can be predicted in simplified manner by Wetzel-Kramers- Brillouin (WKB) approximation as follows:

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|q|\hbar(E_g + \Delta\phi)} \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}} \right) \,, \tag{4}$$

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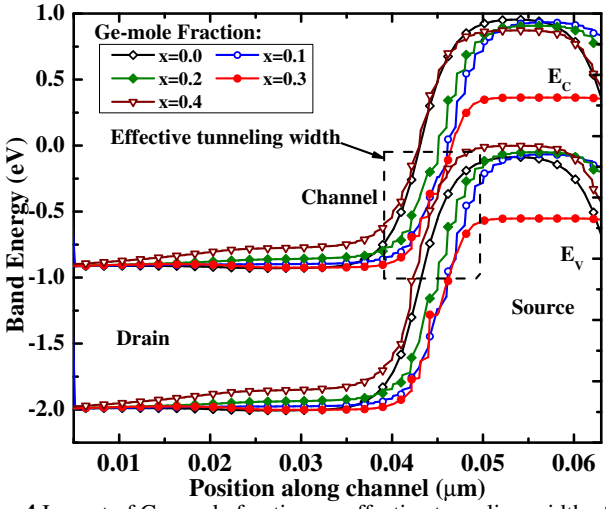

Fig. 4 Impact of Ge- mole fraction on effective tunneling width of applied voltages: V_{GS} = 1.0V, V_{DS} = 1.0V and $V_{gate-aux}$ = 0.0V, respectively.

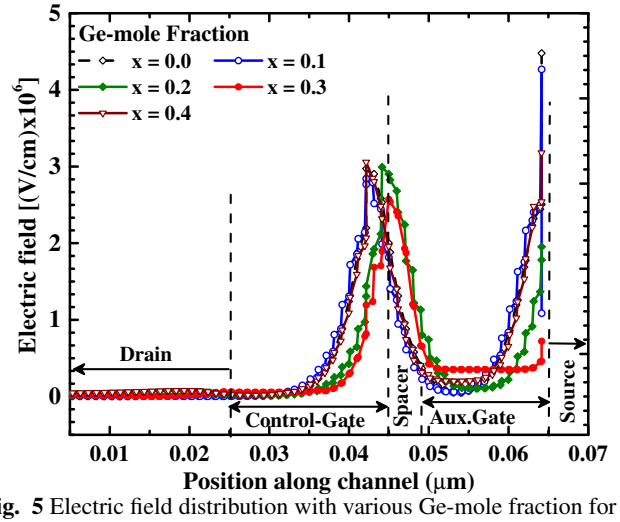

Fig. 5 Electric field distribution with various Ge-mole fraction for same V_{GS} = 1.0V, V_{DS} = 1.0 V with high-K, HfO_2 gate dielectric material gate work function, ϕ_{Gate} = 4.2eV, $\phi_{auxilay}$ = 5.2eV respectively.

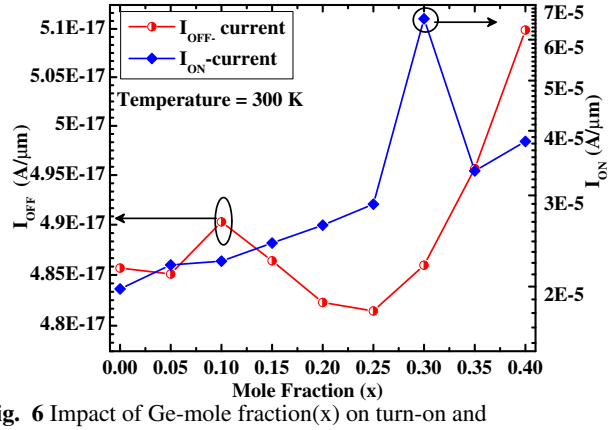

Fig. 6 Impact of Ge-mole fraction(x) on turn-on and off-characteristics on JL-TFET on source: $Si_{1-x}Ge_x$.

where T(E) is the tunneling probability, E_g is the bandgap, q is the universal charge constant, m^* is the effective mass and t_{ox} , t_{Si}, ε_{ox} and ε_{si} are the gate oxide thickness, semiconductor thickness and dielectric constant of oxide and semiconductor materials respectively. The tunneling window $(\Delta\phi)$ in tunneling probability is written as follows[24]:

$$\Delta\phi = E_V^{ch} - E_C^S. \quad (5)$$

Fig.2(a) and Fig.2(b) show the turn-off and turn-on characteristics for the studied HJL-DGTFET respectively. These figures indicates that the turn-on and turn-off characteristics of HJL-DGTFET are governed by the applied gate voltage. The carrier transport in TFET is mainly due to band-to-band tunneling between source and channel region. As shown in Fig.2, only the electrons which has higher energy than the source/channel interface barrier width can enter in channel region from source and get collected at drain node.

4 Results and Discussion

The device used in study has gate length of 20nm and channel thickness of 5nm with uniform doping of $1.0\times10^{18}cm^{-3}$ in the entire device (see Fig.1). The HJL-DGTFET device has two types of gate: control gate and auxiliary gate and corresponding value of work function used in the study for them is 4.2eV and 5.2eV. The device physics of HJL-DGTFET is different from conventional bulk MOSFET. The current conduction in HJL-DGTFET device is entirely dependent on the tunneling width and tunneling width dependence on the device parameters such as t_{ox}, ε_{ox}, band gap (E_g) and effective mass (m^*) is comprehensively presented in this section.

As Ge-mole fraction in $Si_{1-x}Ge_x$ semiconductor increases, the effective tunneling width in the tunneling region at $Si/Si_{1-x}Ge_x$ interface reduces due to the compressive biaxial strain between $Si_{1-x}Ge_x$ and Si. Due to this the tunneling probability increases as a result tunneling current also increases. The tunneling width (λ) variation against the Ge-mole fraction is shown in Fig.4. The impact of germanium mole fraction on the current is shown in Fig.3.

The impact of Ge-mole fraction on internal electric field along the channel is shown in Fig.5. The effective electric filed across the tunneling junction is shown in Fig.5, results improved B2B tunneling current as shown in Fig.3. The electric filed inside tunneling junction also accompanied with rise in tunneling current in OFF-state. The OFF-state (I_{OFF}) and ON-state (I_{ON}) current variation versus Ge-mole fraction for HJL-DGTFET is shown in Fig.6. The, (I_{ON}) and (I_{OFF})-current variation versus Ge-mole fraction illustrates that during device fabrication, Ge-mole fraction in source plays a significant role for optimized device response. Around 30% of Ge-mole frac-

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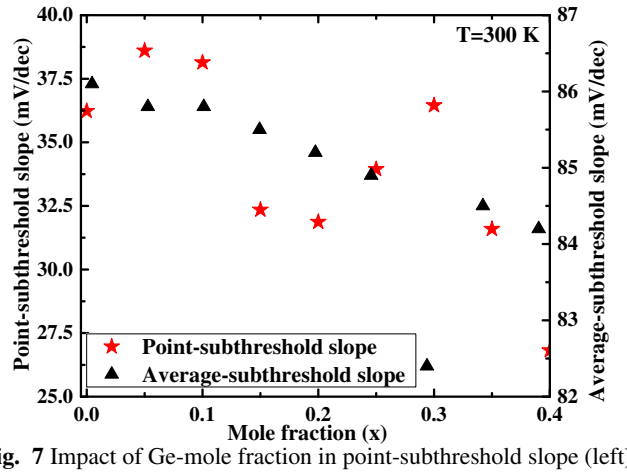

Fig. 7 Impact of Ge-mole fraction in point-subthreshold slope (left) and average subthreshold slope (right).

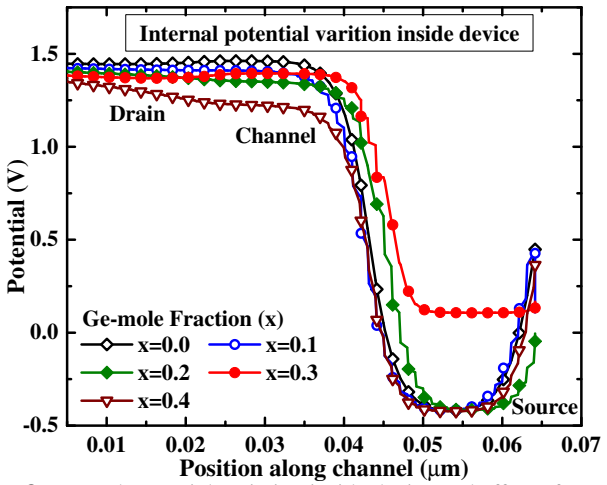

Fig. 8 .Internal potential variation inside device and effect of Ge-mole fraction for applied biasing voltages: V_{GS} = 1.0V, V_{DS} = 1.0V and $V_{G-auxiliary}$ = 0.0V for HfO_2, gate dielectric material with 2nm physical thickness respectively.

tion for the adopted device showing optimized device performance but higher germanium mole fraction (> 30 %) reduces the band to band tunneling. Ge-mole content around 25% to 35% compressive strain gives lowest (I_{OFF})[11]. Due to ultra thin double gate TFET structure, electrons are quantized and quantum confinement results in effective bandgap increase.

Another device characteristics associated with adopted HJL-DGTFET are point subthreshold slope and average subthreshold slope. The value of point subthreshold is calculated by the

$$S_{point} = \left(\frac{dlog_{10}I_{DS}}{dV_{GS}}\right)^{-1}, \qquad (6)$$

where S_{point} is the point subthreshold slope, I_{DS} is the drain current and V_{GS} is the applied gate voltage respectively and

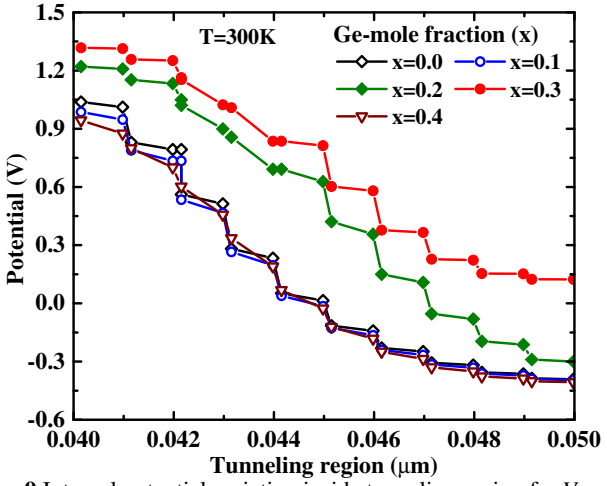

Fig. 9 Internal potential variation inside tunneling region for V_{DS} = 1.0V, V_{GS} = 1.0V, V_{G-aux} = 0.0V with Ge-mole fraction variation.

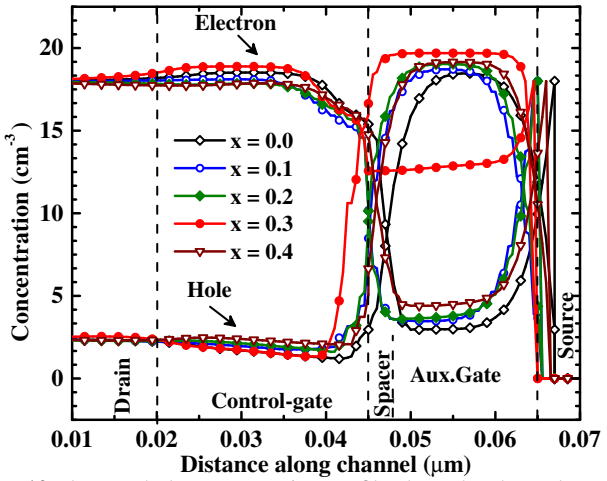

Fig. 10 Electron-hole concentration profile along the channel versus Ge-mole fraction for V_{DS} = 1.0V.

the average subthreshold slope is calculated as follows

$$S_{avg} = \frac{V_T - V_{Goff}}{log_{10}\left(\frac{I_T}{I_{off}}\right)} \approx \frac{V_{DD}}{log_{10}\left(\frac{I_{ON}}{I_{off}}\right)}, \qquad (7)$$

where V_T is the threshold voltage, V_{GOff} is the gate voltage at which drains current starts to rise, I_{off} is the drain current at $V_{GS} = V_{OFF}$ and I_T stands for tunneling current respectively.

The impact of Ge-mole fraction on point subthreshold slope is shown in Fig.7. The reduced point subthreshold with higher content of germanium shows that tunneling current increases with increase in Ge-mole fraction. The reduction in average subthreshold slope with increment in Ge-mole fraction shows the scalable property of power supply voltage (V_{DD}) which in turns reduces the leakage power. The internal potential variation along the channel is shown in Fig.8 and potential varia-

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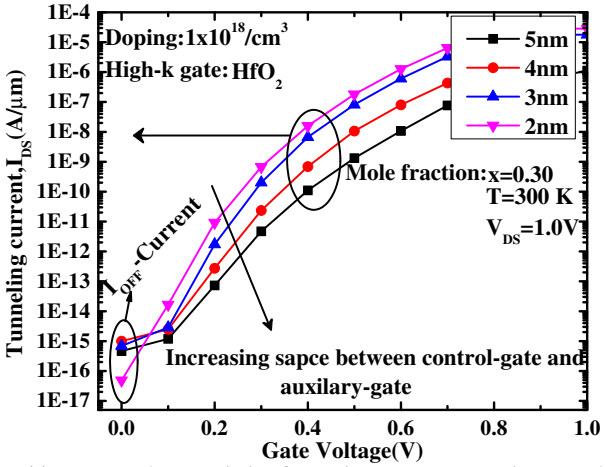

Fig. 11 Turn-on characteristics for various gate spacers in control and auxiliary gate.

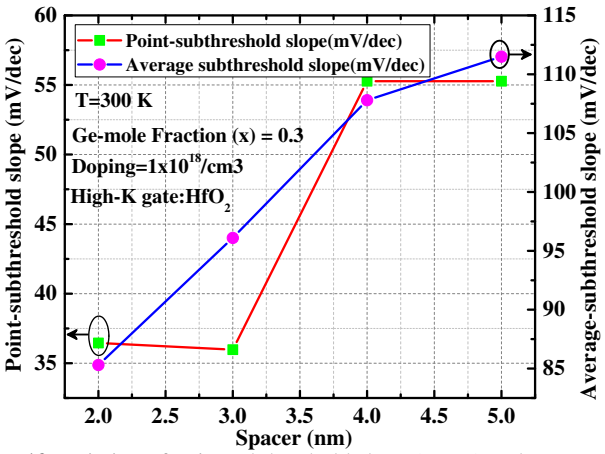

Fig. 12 Variation of point subthreshold slope (S_{point}) and average subthreshold slope ($S_{average}$) with gate spacer.

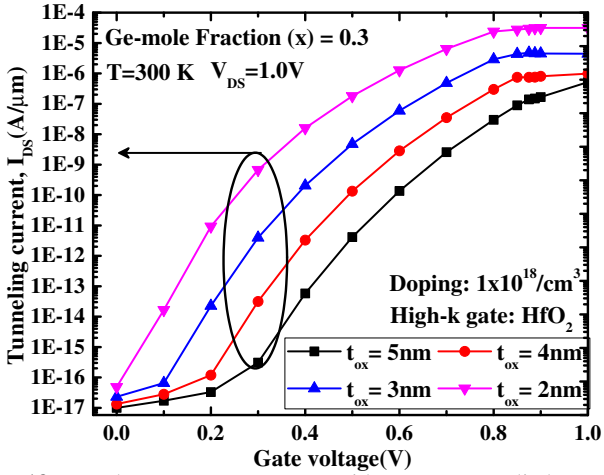

Fig. 13 Tunnel current response, I_{DS} with respect to applied control gate voltage at $V_{G-auxiliary}$ = 0.0V and V_{DS} = 1.0V for different oxide thickness.

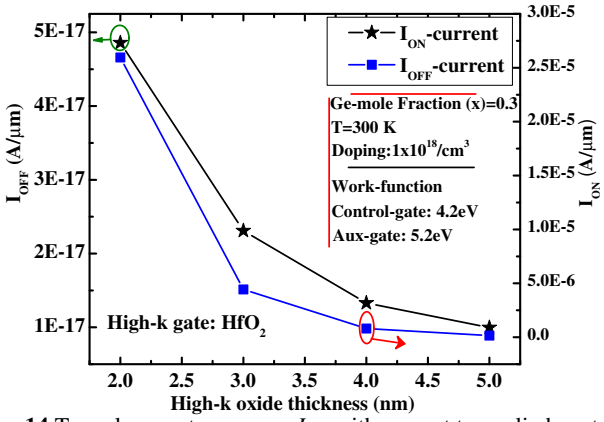

Fig. 14 Tunnel current response, I_{DS} with respect to applied control gate voltage at $V_{G-auxiliary}$ = 0.0V and V_{DS} = 1.0V for different oxide thickness.

tion for tunneling region is shown in Fig.9. The plot in Fig.9 is for on-state condition for Ge-mole fraction of 0.0% to 40% in source for V_{GS} = 1.0V, V_{G-aux} = 0.0V and V_{DS} =1.0V. The internal potential variation is showing similar trend as energy bandgap have with Ge-mole faction. The shift in internal potential with Ge-mole fraction along the channel (see Fig.8 and Fig.9) also shift the electrons and hole concentration in the device as shown in Fig. 10.

The impact of spacer length, oxide thickness and gate dielectric constant on device performance is shown in Figs.11-18. Fig. 11 shows the effect of spacer length variation on the turn-on characteristics of HJL-DGTFET. The contribution of field line passing through the spacer region to the total field lines in the tunneling region varies with the spacer length which in turn affects the tunneling probability. As a result, the on-state current (see Fig.11) as well as subthreshold slope (see Fig.12) vary with the variation in spacer length.

The impact of oxide thickness (t_{ox}) is shown in Figs.13-15. Similar to the conventional MOSFETs, gate oxide thickness plays very crucial role in the tunneling phenomenon through capacitive coupling. The variation in tunneling current with oxide thickness is shown in Fig.13 for Ge-mole fraction of 30%, V_{DS} = 1.0V, V_{G-aux} = 0.0V at T=300K. It shows that thicker gate oxide has lesser impact on the tunneling current than thinner due to the lower capacitive coupling. The variation of t_{ox} also influence the tunneling probability according to the WKB approximation (see Eq (4)) due to modulation in the tunneling width. Thicker gate oxide (t_{ox}) increases the tunneling width (λ) and vice-versa happens for thinner gate oxide as follows:

$$\lambda = \sqrt{\left(\frac{\varepsilon_{si} t_{si} t_{ox}}{\varepsilon_{ox}}\right)} \qquad (8)$$

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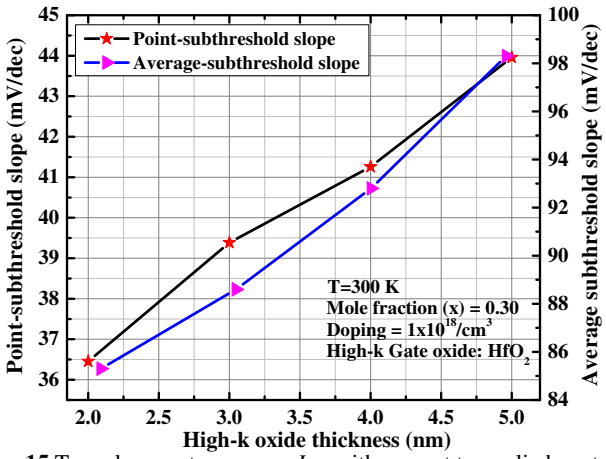

Fig. 15 Tunnel current response, I_{DS} with respect to applied control gate voltage at $V_{G-auxiliary}$ = 0.0V and V_{DS} = 1.0V for different oxide thickness.

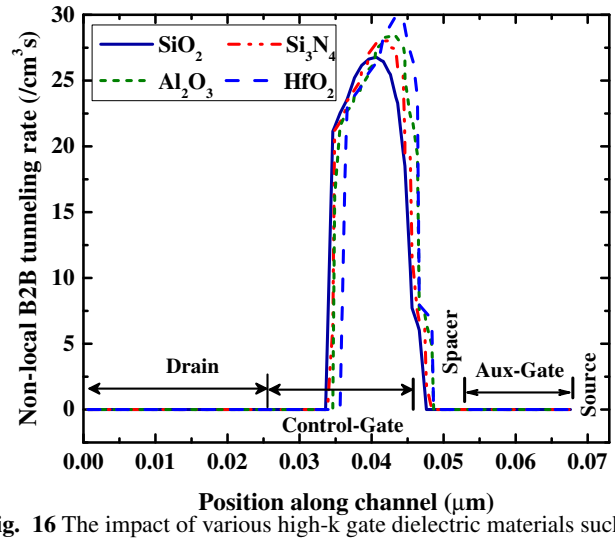

Fig. 16 The impact of various high-k gate dielectric materials such as: SiO_2 (ε_r = 3.9) Si_3N_4 (ε_r = 7.0), Al_2O_3 (ε_r = 9) and HfO_2 (ε_r = 25) upon band-to-band tunneling rate

The reduction in oxide thickness increases on-state current as well as off-state current as shown in Fig.14. The off-state current in thinner gate oxide increases due to increase in the gate leakage current. The decrease in gate oxide thickness also improves the point subthreshold slope as well as the average subthreshold slope due to improvement in on-state current (see Eq. (6) and Eq. (7)) as shown in Fig.15.

Influence of the gate dielectric constant (ε_{ox}) is shown in Fig. 16. From Eq. (8), it is clear that higher value of ε_{ox} (i.e. high-K materials) reduces the tunneling width which in turns improves the non-local tunneling rate (see Fig.16) according to the WKB approximation. The improvement in on-state characteristics with high-K gate oxide materials is shown in Fig.17. The high-k gate dielectric materials also increases the leakage current due to strong coupling between gate and

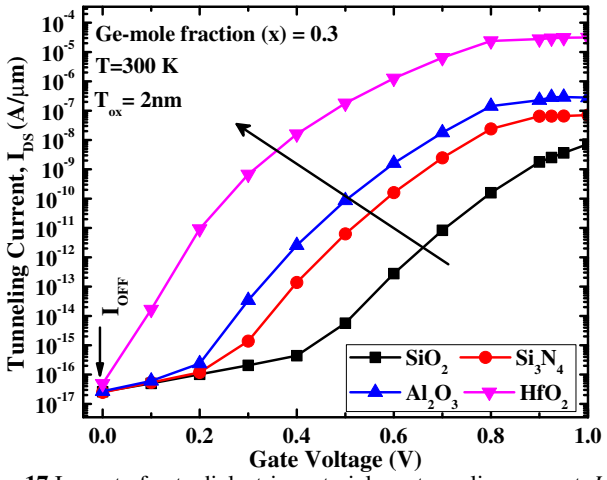

Fig. 17 Impact of gate dielectric materials on tunneling current, I_{DS} for applied terminal voltages: V_{DS} = 1.0V, V_{auxi} = 0.0V with t_{ox} = 2nm.

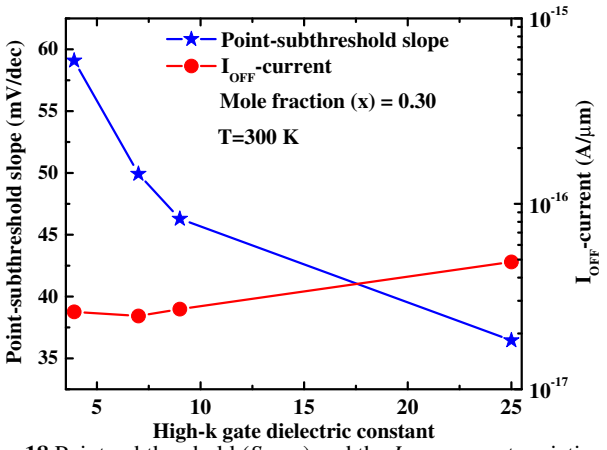

Fig. 18 Point-subthreshold (S_{point}) and the I_{OFF} current variation versus high-K gate dielectric materials at room temperature for V_{DS}= 1.0V, V_{GS} = 1.0, and V_{G-aux} = 0.0V respectively

tunneling region[16]. The adopted HJL-DGTFET shows very weak dependence of leakage current ($I_{OFF} \approx 10^{-16} A/\mu$m to $10^{-17} A/\mu$m) with increase in gate dielectric materials (k=3.9 to 25). The dependency of gate dielectric material on I_{OFF} and point subthreshold slope (S_{point}) is shown in Fig.18. It shows that use of low-k gate dielectric material has poor point subthreshold slope in comparison to the high-K.

5 Conclusions

In this paper, a comprehensive analysis of 20nm double gate HJL-DGTFET is presented. In the analysis, impact of material parameters such as germanium mole fraction, gate oxide thickness, dielectric constant and spacing between the auxiliary and control gate on device performance is presented in detailed . It is observed that Ge-mole fraction plays a significant role in the improvement of HJL-DGTFET performance

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with high-k gate dielectric material. In the study we have found that the device with 30% Ge- mole fraction for 2nm oxide thickness shows very good $I_{OFF} \approx 4.8 \times 10^{-17}$ A/μm, $I_{ON} \approx 6.5 \times 10^{-5} A/\mu$m, and subthreshold slope characteristics subthreshold point, $S_{Piont} \approx 36.4 mV/dec$ and $S_{average} \approx 82.4 mV/dec$ with V_{DS} = 1.0 V.

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